START

CHAPTER 4

BIPOLAR JUNCTION TRANSISTORS

OUTLINE

OBJECTIVES

- Explore the basic dc bias configurations for the bipolar junction transistor.
- Develop an understanding of the relationship between I_C, I_B, and I_E.
- Understand the transistor modes of operation and how they apply to circuit operation.
- Understand the characteristics of basic transistor curves.
- Explore the use of a BJT transistor switch and understand how to bias the transistor switch for use in a circuit.

4–1 INTRODUCTION

The workhorse of modern electronic circuits, both discrete and integrated analog and digital, is the *transistor*. The importance of this versatile device stems from its ability to produce *amplification*, or *gain*, in a circuit. We say that amplification has been achieved when a small variation in voltage or current is used to create a large variation in one of those same quantities, and this is the fundamental goal of most electronic circuits. As a means for creating gain, the transistor is in many ways analogous to a small valve in a large water system: By expending a small amount of energy (turning the valve), we are able to control—increase or decrease—a large amount of energy (in the flow of a large quantity of water). When a device such as a transistor is used to create gain, we supply a small signal to it and refer to that as the *input;* the large current or voltage variations that then occur at another point in the device are referred to as the *output*.

The two most important kinds of transistors are the *bipolar junction* type and the *field-effect* type. The bipolar junction transistor (BJT) is so named (*bi polar*—two polarities) because of its dependence on both holes and electrons as charge carriers. We will study the theory and applications of "bipolars" in this and the next chapter, and devote equal time to field-effect transistors (FETs), which operate under completely different principles, in Chapter 5.

We should note that bipolars are studied first for historical reasons, and because the theory of these devices follows naturally from a study of *pn* junctions. Their precedence in our study should in no way imply that they are of greater importance than field-effect transistors. Bipolars were the first kind of transistors to be widely used in electronics, and they are still an important segment of the semiconductor industry. Most people in the industry still use the word *transistor* (as we shall) with the understanding that a bipolar transistor is meant. However, field-effect technology has now evolved to the point where FETs are used in greater numbers than BJTs in integrated circuits for digital and analog applications.

4–2 THEORY OF BJT OPERATION

A bipolar junction transistor is a specially constructed, *three-terminal* semiconductor device containing *two pn* junctions. It can be formed from a bar of material that has been doped in such a way that it changes from *n* to *p* and back to *n*, or from *p* to *n* and back to *p*. In either case, a junction is created at each of the two boundaries where the material changes from one type to the other. Figure 4–1 shows the two ways that it is possible to alternate material types and thereby obtain two junctions.

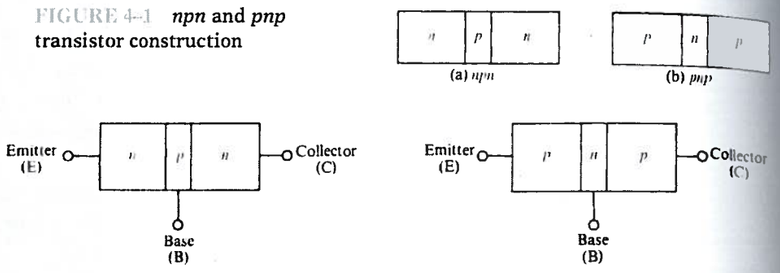


FIGURE 4–1 *npn* and *pnp* transistor construction

FIGURE 4–2 Base, emitter, and collector terminals of *npn* and *pnp* transistors

When a transistor is formed by sandwiching a single *p* region between two *n* regions, as shown in Figure 4–1(a), it is called an *npn* type. Figure 4–1(b) shows the *pnp* type, containing a single *n* region between two *p* regions.

The middle region of each transistor type is called the *base* of the transistor. Of the remaining two regions, one is called the *emitter* and the other is called the *collector* of the transistor. Let us suppose that terminals are attached to each region so that external electrical connections can be made between them. (In integrated circuits, no such accessible terminals may be provided, but it is still possible to identify the base, emitter, and collector and to form conducting paths between those regions and other internal components.) Figure 4–2 shows terminals attached to the regions of each transistor type. The terminals are labeled according to the region to which they connect.

The physical appearance of an actual transistor bears little resemblance to the figures we have shown so far. However, these kinds of diagrams are very helpful in understanding transistor theory, and Figures 4–1 and 4–2 are representative of actual transistors in at least one respect: The base region is purposely shown *thinner* than either the emitter or collector region. For reasons that will become evident soon, the base region in an actual transistor is made even thinner in proportion to the other regions than is depicted by the figures. Also, the base region is much more lightly doped than the other regions.* Both these characteristics of the base are important for the transistor to be a useful device and to perform what is called normal "transistor action."

For the sake of clarity, we will continue our discussion of transistor theory in terms of the *npn* type only. The underlying theory is equally applicable to the *pnp* type and can be "translated" for *pnp*s simply by changing each carrier type mentioned in connection with *npn*s and reversing each voltage polarity. To obtain normal transistor action, it is necessary to bias both *pn* junctions by connecting dc voltage sources across them. Figure 4–3 illustrates the correct bias for each junction in the *npn* transistor. In the figure, we show the result of biasing each junction separately, while in practice both junctions will be biased simultaneously by one external circuit, as will be described presently.

As shown in Figure 4–3(a), the emitter–base junction is forward biased by the dc source labeled V_{EE}. Note that the *n*egative terminal of V_{EE} is connected to the *n* side of the *np* junction, as required for forward bias. Consequently, there is a substantial flow of diffusion current across the junction due to the flow of the majority carriers (electrons) from the *n*-type emitter. This action is exactly that which we discussed in connection with a forward-biased *pn*

*In integrated circuits, the emitter is usually heavily doped (n^+) material. Most integrated-circuit BJTs are of the *npn* type.

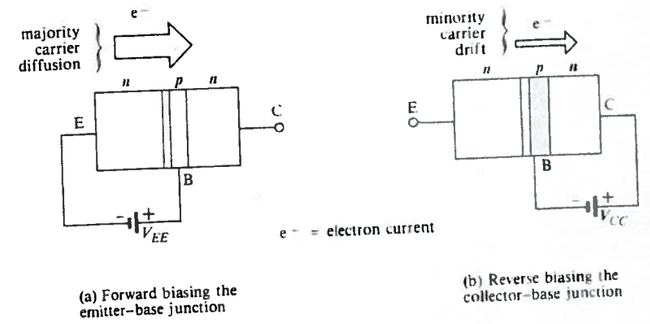


FIGURE 4–3 Biasing the two *pn* junctions in an *npn* transistor

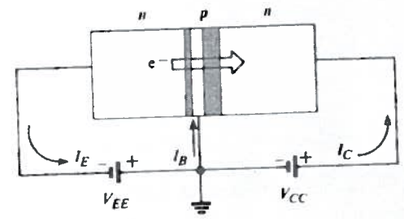


FIGURE 4–4 The *npn* transistor with both bias sources connected

junction in Chapter 2. The depletion region at this junction is made narrow by the forward bias, as also described in Chapter 2. The width of the base region is exaggerated in the figure for purposes of clarity. When the majority electrons diffuse into the base, they become minority carriers in that *p*-type region. We say that minority carriers have been *injected* into the base.

Figure 4–3(b) shows that the collector-base junction is reverse biased by the dc source labeled V_{CC}. The positive terminal of V_{CC} is connected to the *n*-type collector. As a result, the depletion region at this junction is widened, and the only current that flows from base to collector is due to the minority electrons crossing the junction from the *p*-type base. Recall from Chapter 2 that *minority* carriers readily cross a reverse-biased junction under the influence of the electric field, and they constitute the flow of reverse current in the junction:

Figure 4–4 shows the *npn* transistor the way it is biased for normal operation, with both dc sources V_{EE} and V_{CC} connected simultaneously. Note in the figure that the negative terminal of V_{CC} is connected to the positive terminal of V_{EE} and that both of these are joined to the base. The base is then the "ground," or common point of the circuit, and can therefore be regarded as being at 0 V. The emitter is negative *with respect to the base*, and the collector is positive *with respect to the base*. These are the conditions we require in order to forward bias the emitter–base junction and to reverse bias the collector–base junction.

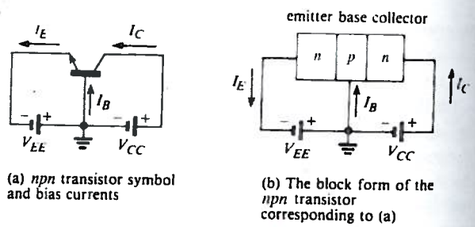
Because the base region is very thin and is lightly doped relative to the heavily doped emitter (so there are relatively few holes in it), very few of the electrons injected into the base from the emitter recombine with holes. Instead, they diffuse to the reverse-biased base–collector junction and are swept across that junction under the influence of the electric field established by V_{CC}. Remember, again, that the electrons injected into the base are the minority carriers there, and that minority carriers readily cross the reverse-biased junction. We conclude that electron flow constitutes the dominant current type in an *npn* transistor. For a *pnp* transistor, in which everything is "opposite," hole current is the dominant type.

Despite the fact that most of the electrons injected into the base cross into the collector, a few of them do combine with holes in the base. For each electron that combines with a hole, an electron leaves the base region via the base terminal. This action creates a very small base current, about 2% or less of the electron current from emitter to collector. As we shall see, the smaller this percentage, the more useful the transistor is in practical applications.

Note in Figure 4–4 that arrows are drawn to indicate the direction of *conventional* current in the *npn* transistor. Of course, each arrow points in the opposite direction from the electron flows that we have described. Conventional current flowing from V_{CC} into the collector is called *collector current* and designated I_C. Similarly, current into the base is I_B, the *base current*, and current from V_{EE} into the emitter is *emitter current*, I_E. Figure 4–5(a) shows the standard electronic symbol for an *npn* transistor, with these currents labeled alongside. Figure 4–5(b) shows the same block form of the *npn* that we have shown earlier and is included as an aid for relating the physical device to the symbol. Figure 4–6 shows the standard symbol for a *pnp* transistor and its equivalent block form. Comparing Figures 4–5 and 4–6, we note first that the emitter of an *npn* transistor is represented by an arrow pointing out from the base, whereas the emitter of a *pnp* transistor is shown as an arrow pointing into the base. It is easy to remember this distinction by thinking of the arrow as pointing in the direction of conventional current flow, out of or into the emitter of each type of transistor. We further note that the polarities of the bias sources for the *pnp* transistor, V_{EE} and V_{CC}, are the opposite of those for the *npn* transistor. In other words, the positive and negative terminals of each source in Figure 4–6 are the reverse of those in Figure 4–5. These polarities are, of course, necessary in each case to maintain the forward and reverse biasing of the junctions, as we have described. Note, for example, that the negative terminal of V_{CC} is connected to the *p*-type collector of the *pnp* transistor. Recapitulating, here is the all-important universal rule for biasing transistors for normal operation (memorize it!): *The emitter–base junction must be forward biased, and the collector–base junction must be reverse biased.*

To emphasize and clarify an important point concerning transistor currents, Figure 4–7 replaces each type of transistor by a single block and shows the directions of currents entering and leaving each. Applying

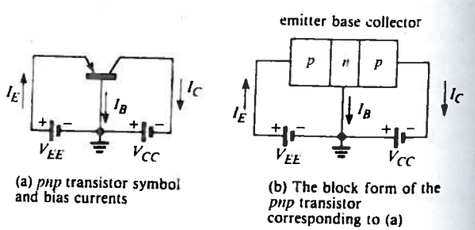
FIGURE 4–5 Equivalent *npn* transistor diagrams



(a) *npn* transistor symbol and bias currents

(b) The block form of the *npn* transistor corresponding to (a)

FIGURE 4–6 Equivalent *pnp* transistor diagrams



(a) *pnp* transistor symbol and bias currents

(b) The block form of the *pnp* transistor corresponding to (a)

FIGURE 4–7 Each transistor type is replaced by a single block to highlight current flows in and out of the devices

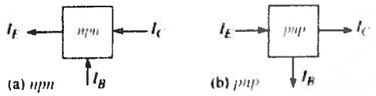
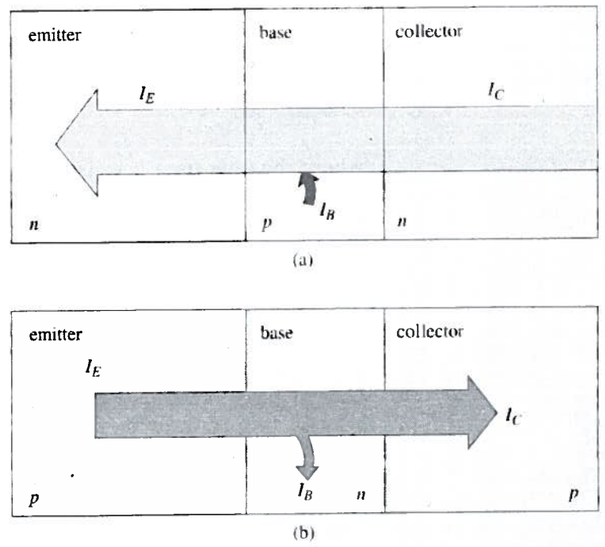


FIGURE 4–8 Graphical depiction of the relationships among the emitter, base, and collector currents



Kirchhoff's current law to each of Figures 4–7(a) and (b), we immediately obtain this important relationship, applicable to both *npn* and *pnp* transistors:

$$I_E = I_C + I_B \tag{4–1}$$

that is graphically depicted in Figure 4–8.

I_{CBO} Reverse Current

Recall from Chapter 2 that a small reverse current flows across a *pn* junction due to *thermally* generated minority carriers that are propelled by the barrier potential. When the junction is reverse biased, this reverse current increases slightly. For moderate reverse-bias voltages, the reverse current reaches its saturation value, I_s. Because the collector–base junction of a transistor is reverse biased, there is likewise a reverse current due to thermally generated carriers. Of course this "reverse" current, in the context of a transistor, is in the same direction as the main (collector) current flowing through the device due to the injection of minority carriers into the base. The total collector current is, therefore, the *sum* of these two components: the injected minority carriers and the thermally generated minority carriers.

Suppose that the external connections between the base and emitter are left open and that the collector–base junction has its normal reverse bias, as shown in Figure 4–9 (see also Figure 4–3). Because the emitter is open, there can be no carriers injected into the base. Consequently, the only current that flows must be that "reverse" component due to thermally generated carriers. This current is designated I_{CBO}, the Collector-to-Base

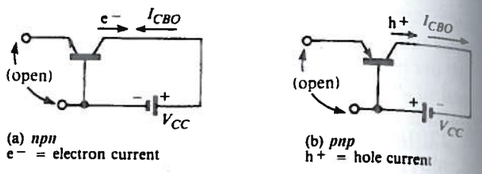


FIGURE 4–9 I_{CBO} is the collector current that flows when the emitter is open

current, with the emitter *O*pen. Therefore, in normal operation, with the emitter circuit connected, the total collector current is expressed as

$$I_C = \alpha I_E + I_{CBO} \tag{4–2}$$

where the important transistor parameter *alpha* is defined as the ratio of the collector current resulting from carrier injection to the total emitter current:

$$\alpha = \frac{I_{C(INJ)}}{I_E} \tag{4–3}$$

Thus, α measures the portion of the emitter current that "survives," after passage through the base, to become collector current. Clearly, α will always be less than 1, because some of the emitter current is drained off in the base through recombinations. Generally speaking, the greater the value of α (the closer it is to 1), the better the transistor, from the standpoint of many practical applications that we will explore later. In other words, we want a transistor to be constructed so that its base current is as small as possible, because that makes I_C close to I_E and α close to 1. Typical transistors have values of α that range from 0.95 to 0.995.

Equation 4–2 states that the total collector current is that portion of the emitter current that makes it through the base (αI_E) plus the thermally generated collector current (I_{CBO}).

In modern transistors, particularly silicon, I_{CBO} is so small that it can be neglected for most practical applications. Remember that I_{CBO} is exactly the same as the reverse diode current we discussed in Chapter 2. We saw that its theoretical value, as a function of temperature and voltage, is given by equation 2–3, and that it is quite sensitive to temperature variations. Because the collector–base junction in a transistor is normally reverse biased by at least a volt or so, the theoretical value of I_{CBO} is for all practical purposes equal to its saturation value (I_s, in Chapter 2). Remember that I_s approximately doubles for every 10°C rise in temperature, so we can say the same about I_{CBO} in a transistor. This sensitivity to temperature can become troublesome in some circuits if high temperatures and large power dissipations are likely. We will explore those situations in more detail later.

We should also remember that the theoretical value of I_{CBO}, like reverse diode current, is usually much smaller than the reverse *leakage* current that flows across the surface. In silicon transistors, this surface leakage may so completely dominate the reverse current that temperature-related increases in I_s remain negligible. In fact, it is conventional in most texts and product literature to refer to I_{CBO} as the (collector-to-base) *leakage current*.

Because I_{CBO} is negligibly small in most practical situations, we can set it equal to 0 in equation 4–2 and obtain the good approximation

$$I_C \approx \alpha I_E \tag{4–4}$$

and

$$\alpha \approx \frac{I_C}{I_E} \tag{4–5}$$

EXAMPLE 4–1

The emitter current in a certain *npn* transistor is 8.4 mA. If 0.8% of the minority carriers injected into the base recombine with holes and the leakage current is 0.1 μA, find (1) the base current, (2) the collector current, (3) the exact value of α, and (4) the approximate value of α, neglecting I_{CBO}.

Solution

1. I_B = (0.8% of I_E) = (0.008)(8.4 mA) = 67.2 μA.
2. From equation 4–1, $I_C = I_E - I_B$ = 8.4 mA − 0.0672 mA = 8.3328 mA.
3. From equation 4–2, $\alpha I_E = I_C - I_{CBO}$ = 8.3328 × 10^{-3}A − 10^{-7}A = 8.3327 mA. By equation 4–3, α = (8.3327 mA)/(8.4 mA) = 0.9919881.
4. By approximation 4–5, $\alpha \approx I_C/I_E$ = (8.3328 mA)/(8.4 mA) = 0.992.

For the conditions of this example, we see that the exact and approximate values of α are so close that the difference between them can be entirely neglected.

4–3 COMMON-BASE CHARACTERISTICS

In our introduction to the theory of transistor operation, we showed a bias circuit (Figure 4–4) in which the base was treated as the ground, or "common" point of the circuit. In other words, all voltages (collector-to-base and emitter-to-base) were *referenced* to the base. This bias arrangement results in what is called the *common-base* (CB) configuration for the transistor. It represents only one of three possible ways to arrange the external circuit to achieve a forward-biased base-to-emitter junction and a reverse-biased collector-to-base junction, because any one of the three terminals can be made the common point. We will study the other two configurations in later discussions.

The significance of having a common point in a transistor circuit is that it gives us a single reference for both the *input* voltage to the transistor and the *output* voltage. In the CB configuration, the emitter–base voltage is regarded as the input voltage and the collector–base voltage is regarded as the output voltage. See Figure 4–10. Notice the reference for V_{EB} and V_{CB} where standard double-subscript notation means "voltage at first subscript with respect to second subscript." For normal transistor action, V_{EB} is positive for *pnp* and negative for *npn*. On the other hand, V_{CB} is negative for *pnp* and positive for *npn*.

In our analysis of the CB configuration, the "input" voltage will be the emitter–base *bias* voltage (V_{EB}), and the "output" voltage will be the collector–base bias voltage (V_{CB}). In Chapter 7, we will adopt a more realistic viewpoint in which we will regard small (ac) variations in the emitter–base and collector–base voltages as the input and output, respectively. For the time being, we will concern ourselves only with the effects of changes in V_{EB} and V_{CB} on the behavior of the transistor. Do not be confused by the fact that the "input" current in the *npn* circuit (Figure 4–10(a)) flows *out* of the

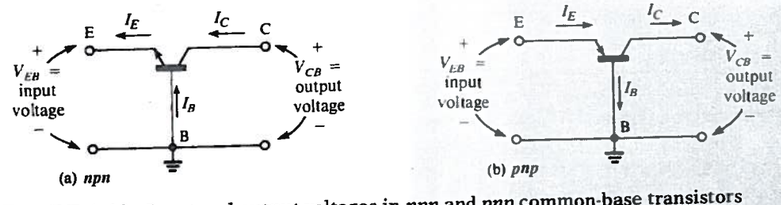


FIGURE 4–10 Input and output voltages in *npn* and *pnp* common-base transistors

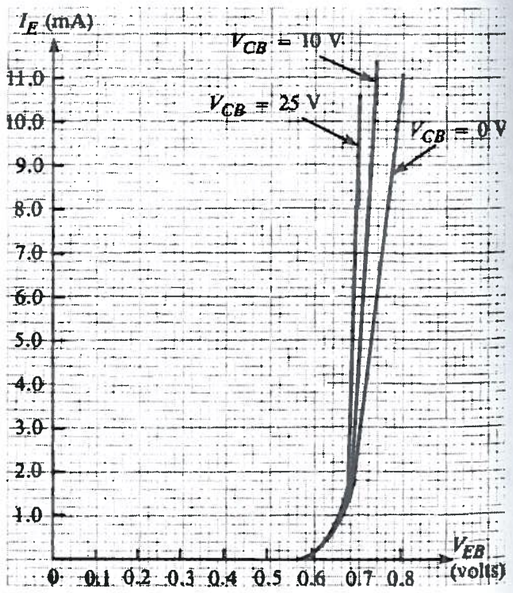
emitter. Again, it will be small changes in the magnitude of I_E that we will ultimately regard as the "input."

Our objective now is to learn how the input and output voltages and the input and output currents are related to each other in a CB configuration. Toward that end, we will develop sets of characteristic curves called *input* characteristics and *output* characteristics. The input characteristics show the relation between input current and input voltage *for different values of output voltage*, and the output characteristics show the relation between output current and output voltage *for different values of input current*. As these statements suggest, there is in a transistor a certain *feedback* (the output voltage) that affects the input, and a certain "feedforward" (the input current) that affects the output.

Common-Base Input Characteristics

Let us begin with a study of the CB input characteristics of a typical *npn* transistor. Because the input is across the forward-biased base-to-emitter junction, we would expect a graph of input current (I_E) versus input voltage (V_{EB}) to resemble that of a forward-biased diode. That is indeed the case. However, the exact shape of this I_E–V_{EB} curve will, as we have already hinted, depend on the reverse-biasing output voltage, V_{CB}. The reason for this dependency is that the greater the value of V_{CB}, the more readily minority carriers in the base are swept through the base-to-collector junction. (Remember that the reverse-biasing voltage enhances such current.) The increase in emitter-to-collector current resulting from an increase in V_{CB} means that the (input) emitter current will be greater for a given value of (input) base-to-emitter voltage. Figure 4–11 shows a typical set of input characteristics in which this feedback effect can be discerned. Figure 4–11 is our first example of a *family* of transistor curves, a very useful way to display transistor behavior graphically and one that can provide rewarding insights if studied carefully. Although characteristic curves are seldom used in actual design or analysis

FIGURE 4–11 Common-base input characteristics (*npn*)



problems, they convey a wealth of information, and we will see many more of them in the future. Each set should be scrutinized and dwelled upon at length. Try to visualize how currents and/or voltages change when one quantity is held constant and the others are varied. Note that a family of curves can show the relationships among *three* variables: two represented by the axes, and the third represented by each curve. In Figure 4–11, each curve corresponds to a different value of V_{CB} and therefore each shows how emitter current varies with base-to-emitter voltage for a fixed value of V_{CB}. A good way to view this family is to think of an experiment in which the reverse-biasing voltage V_{CB} is fixed and a set of measurements of I_E is made for different settings of V_{EB}. Plot these results, and then set V_{CB} to a new value and repeat the measurements. Each time V_{CB} is set to a new value, a new curve is obtained.

Note in Figure 4–11 that each curve resembles a forward-biased diode characteristic, as expected. For a given value of V_{EB}, it can be seen that I_E increases with increasing V_{CB}. This variation has already been explained in terms of the way V_{CB} promotes minority carrier flow. We see in the figure that there is actually little difference in the shapes of the curves as V_{CB} is changed over a fairly wide range. For that reason, the effect of V_{CB} on the input is often neglected in practical problems. An "average" forward-biased diode characteristic is assumed.

The CB input characteristics for a *pnp* transistor will of course have the same general appearance as those shown for an *npn* in Figure 4–11. However, in a *pnp* transistor, a forward-biasing input voltage is positive when measured *from* emitter *to* base. Some data sheets show negative values for *pnp* voltages and/or currents because these quantities have directions that are the opposite of the corresponding *npn* quantities. For example, if the horizontal axis in Figure 4–11 were labeled V_{EB} for a *pnp* transistor, then all scale values would be negative. These sign conventions (rather, this *lack* of consistency) can be confusing but can always be resolved by remembering the fundamental rule for transistor bias: base–emitter forward and base–collector reverse. Finally, we should mention that some authors and some data sheets refer to the CB input characteristics as the *emitter characteristics* of a transistor.

EXAMPLE 4–2

The transistor shown in Figure 4–12 has the characteristic curves shown in Figure 4–11. When V_{CC} is set to 25 V, it is found that I_C = 8.94 mA.

1. Find the α of the transistor (neglecting I_{CBO}).
2. Repeat if I_C = 1.987 mA when V_{CC} is replaced by a short circuit to ground.

Solution

1. In Figure 4–12, we see that V_{BE} = 0.7 V. From Figure 4–11, the vertical line corresponding to V_{BE} = 0.7 V intersects the V_{CB} = 25 V curve at I_E = 9.0 mA. Therefore, $\alpha \approx I_C/I_E$ = (8.94 mA)/(9.0 mA) = 0.9933.
2. When V_{CC} is replaced by a short circuit, we have V_{CB} = 0. From Figure 4–11, I_E = 2 mA at V_{CB} = 0 V and V_{BE} = 0.7 V. Therefore, $\alpha \approx I_C/I_E$ = (1.987 mA)/(2.0 mA) = 0.9935.

FIGURE 4–12 (Example 4–2)

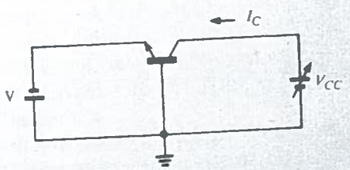
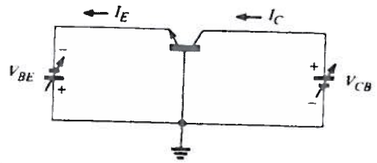


FIGURE 4–13 An experiment that could be used to produce the output characteristics shown in Figure 4–14



I_E	V_{CB}	I_C
1 mA	−1	
1 mA	0	
1 mA	5	
1 mA	10	
1 mA	15	
1 mA	20	

I_E	V_{CB}	I_C
2 mA	−1	
2 mA	0	
2 mA	5	
2 mA	10	
2 mA	15	
2 mA	20	

— etc. —

I_E	V_{CB}	I_C
9 mA	−1	
9 mA	0	
9 mA	5	
9 mA	10	
9 mA	15	
9 mA	20	

1. With V_{CB} set to −1 V, adjust V_{BE} to obtain I_E = 1 mA. Measure and record I_C.
2. Increase V_{CB} positively in small steps, each time measuring I_C. Adjust V_{BE} as necessary to maintain the original value of I_E. Continue until V_{CB} has reached 20 V. Plot I_C versus V_{CB}.
3. Repeat step 1, with V_{BE} adjusted to produce a new, slightly larger value of I_E. Then repeat step 2.

   Repeat step 3 until the fixed value of I_E has reached 9 mA.

Common-Base Output Characteristics

Consider now an experiment in which the collector (output) current is measured as V_{CB} (the output voltage) is adjusted for fixed settings of the emitter (input) current. Figure 4–13 shows a schematic diagram and a procedure that could be used to conduct such an experiment on an *npn* transistor. Understand that Figure 4–13 does not represent a practical circuit that could be used for any purpose other than investigating transistor characteristics. Practical transistor circuits contain more resistors and have input and output voltages that are different from the dc bias voltages. However, at this point in our study of transistor theory, we are interested in the *transistor* itself. We are using characteristic curves to gain insights into how the voltages and currents relate to each other in the *device*, rather than in the external circuit. Once we have gleaned all the device information we can from studying characteristic curves, we will have a solid understanding of what a transistor really is and can proceed to study practical circuits. When I_C is plotted versus V_{CB} for different values of I_E, we obtain the family of curves shown in Figure 4–14: the *output* characteristics for the CB configuration. A close examination of these curves will reveal some new facts about transistor behavior.

We note first in Figure 4–14 that each curve starts at $I_C = 0$ and rises rapidly for a small positive increase in V_{CB}. In other words, I_C increases rapidly just as V_{CB} begins to increase slightly beyond its initial negative value. Since each curve represents a fixed value of I_E, this means that while I_C is increasing, the ratio I_C/I_E must also be increasing. But I_C/I_E equals α, so the implication is that the value of α for a transistor is not constant. Alpha starts at 0 and increases as V_{CB} increases. The reason for this fact is that a very small portion of the emitter current is able to enter the collector region until the reverse-biasing voltage V_{CB} is allowed to reach a value large enough to propel all carriers across the junction. When V_{CB} is negative, the junction is actually

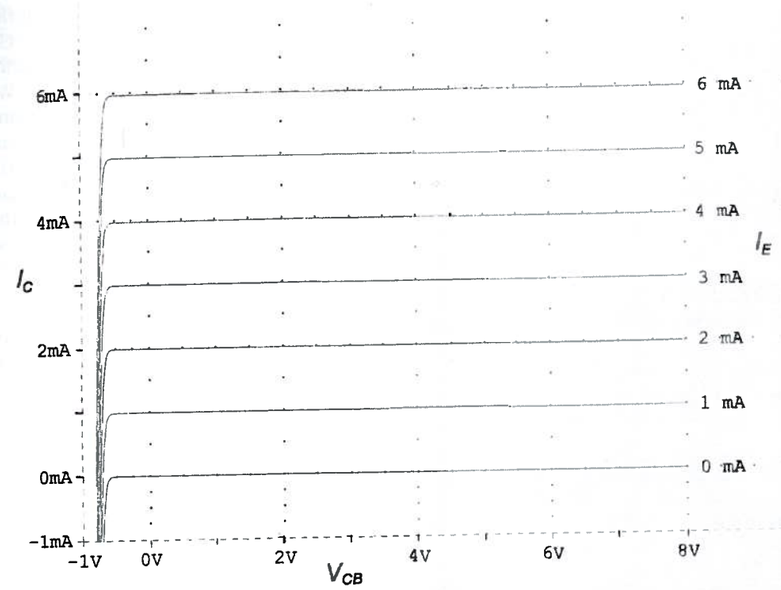


FIGURE 4–14 Common-base output characteristics (*npn*). Note that the negative V_{CB} scale is expanded.

forward biased, and minority carrier flow is inhibited. The proportion of the carriers that are swept across the junction (α) depends directly on the value of V_{CB} until V_{CB} no longer forward biases the junction. The portion of the plot where V_{CB} is negative is called the *saturation region* of the transistor. By definition (no matter what the transistor configuration), a transistor is *saturated* when *both* its collector-to-base junction *and* emitter-to-base junction are forward biased.

Once V_{CB} reaches a value large enough to ensure that a large portion of carriers enter the collector (close to 0 in Figure 4–14), we see that the curves more or less level off. In other words, for a fixed emitter current, the collector current remains essentially constant for further increases in V_{CB}. Note that this essentially constant value of I_C is, for each curve, very nearly equal to the value of I_E represented by the curve. In short, the ratio I_C/I_E, or α, is very close to 1 and is essentially constant. These observations correspond to what we had previously assumed about the nature of α, and the region of the plot where this is the case is called the *active region*. In its active region, a transistor exhibits those "normal" properties (transistor action) that we have associated with a forward-biased emitter–base junction and a reverse-biased collector–base junction. Apart from some special digital-circuit applications, a transistor is normally operated (used) in its active region. Note that we can detect a slight rise in the curves as they proceed to the right through the active region. Each curve of constant I_E approaches a horizontal line for which I_C is almost equal to I_E, implying that I_E approaches I_C, and that α approaches 1, for increasing V_{CB}. This we attribute to the increased number of minority carriers swept into the collector, which increases the collector current, as the reverse-biasing value of V_{CB} is increased.

There is one other region of the output characteristics that deserves comment. Note that the curve corresponding to $I_E = 0$ is very close to the $I_C = 0$

line. When the emitter current is made 0 (by opening the external emitter circuit), no minority carriers are injected into the base. Under those conditions, the only collector current that flows is the very small leakage current, I_{CBO}, as we have previously described (see Figure 4–9). With the scale used to plot the output characteristics in Figure 4–14, a horizontal line corresponding to $I_C = I_{CBO}$ coincides with the $I_C = 0$ line, for all practical purposes. The region of the output characteristics lying below the $I_E = 0$ line is called the *cutoff* region because the collector current is essentially 0 (cut off) there. A transistor is said to be in the cutoff state when *both* the collector–base and emitter–base junctions are reverse biased. Except for special digital circuits, a transistor is not normally operated in its cutoff region.

EXAMPLE 4–3

A certain *npn* transistor has the CB input characteristics shown in Figure 4–11 and the CB output characteristics shown in Figure 4–14.

1. Find its collector current when $V_{CB} = 10\,\text{V}$ and $V_{BE} = 0.7\,\text{V}$.
2. Repeat when $V_{CB} = 5\,\text{V}$ and $I_E = 5.5\,\text{mA}$.

Solution

1. From Figure 4–11, we find $I_E = 4\,\text{mA}$ at $V_{BE} = 0.7\,\text{V}$ and $V_{CB} = 10\,\text{V}$. In Figure 4–14, the $I_E = 4\,\text{mA}$ curve runs just below $I_C = 4\,\text{mA}$. The collector current under these conditions is practically 4 mA, independent of V_{CB}.
2. The conditions given require that we *interpolate* the output characteristics along the vertical line $V_{CB} = 5\,\text{V}$ between $I_E = 5\,\text{mA}$ and $I_E = 6\,\text{mA}$. The value of I_C that is halfway between the $I_E = 5\,\text{mA}$ and $I_E = 6\,\text{mA}$ curves is approximately 5.5 mA. Note that high accuracy is not possible when using characteristic curves in this way. In most practical situations, we could simply assume that $I_C = I_E$ without seriously affecting the accuracy of other computations.

Breakdown

As is the case in a reverse-biased diode, the current through the collector–base junction of a transistor may increase suddenly if the reverse-biasing voltage across it is made sufficiently large. This increase in current is typically caused by the avalanching mechanism already described in connection with diode breakdown. However, in a transistor it can also be the result of a phenomenon called *punch through*. Punch through occurs when the reverse bias widens the collector–base depletion region to the extent that it meets the base-emitter depletion region. This joining of the two regions effectively shorts the collector to the emitter and causes a substantial current flow. Remember that the depletion region extends farther into the lightly doped side of a junction and that the base is more lightly doped than the collector. Furthermore, the base is made very thin, so the two junctions are already relatively close to each other. Punch through can be a limiting design factor in determining the doping level and base width of a transistor. Figure 4–15 shows how the CB output characteristics appear when the effects of breakdown are included. Note the sudden upward swing of each curve at a large value of V_{CB}. The collector-to-base breakdown voltage when $I_E = 0$ (emitter open) is designated BV_{CBO}. As can be seen in Figure 4–15, breakdown occurs at progressively lower voltages for increasing values of I_E.

Although the base–emitter junction is not normally reverse biased, there are practical applications in which it is periodically subjected to reverse bias.

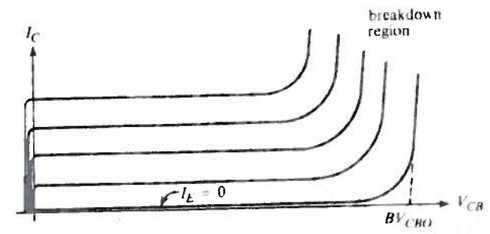


FIGURE 4–15 Common-base output characteristics showing the breakdown region

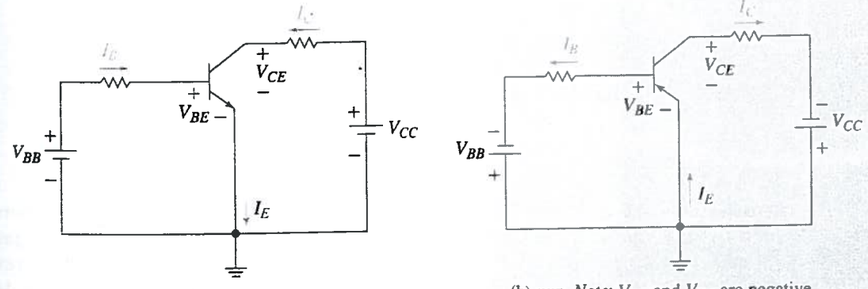
Of course, it too can break down, and its reverse breakdown voltage is usually much less than that of the collector–base junction. Base–emitter breakdown is often destructive, so designers must be aware of the manufacturer's specified maximum reverse base–emitter voltage.

As a final note on transistor operation, we should mention that some transistors can be (and occasionally are) operated in what is called an *inverted* mode. In this mode, the emitter is used as the collector and vice versa. Normally, the emitter is the most heavily doped of the three regions, so unless a transistor is specifically designed for inverted operation, it will not perform well in that mode. The α in the inverted mode, designated α_1, is generally smaller than the α that can be realized in conventional operation.

4–4 COMMON-EMITTER CHARACTERISTICS

The next transistor bias arrangement we will study is called the *common-emitter* (CE) configuration. It is illustrated in Figure 4–16. Note that the external voltage source V_{BB} is used to forward bias the base–emitter junction and the external source V_{CC} is used to reverse bias the collector–base junction. The magnitude of V_{CC} must be greater than V_{BB} to ensure that the collector–base junction remains reverse biased, because, as can be seen in the figure, $V_{CB} = V_{CC} - V_{BB}$. (Write Kirchhoff's voltage law around the loop from the collector, through V_{CC}, through V_{BB}, and back to the collector.) The emitter terminal is, of course, the ground, or common, terminal in this configuration.

Figure 4–17 shows that the input voltage in the CE configuration is the base–emitter voltage and the output voltage is the collector–emitter voltage. The input current is I_B and the output current is I_C. The common-emitter



(a) *npn* (b) *pnp*. *Note:* V_{BE} and V_{CE} are negative for *pnp* transistors.

FIGURE 4–16 Common-emitter (CE) bias arrangements

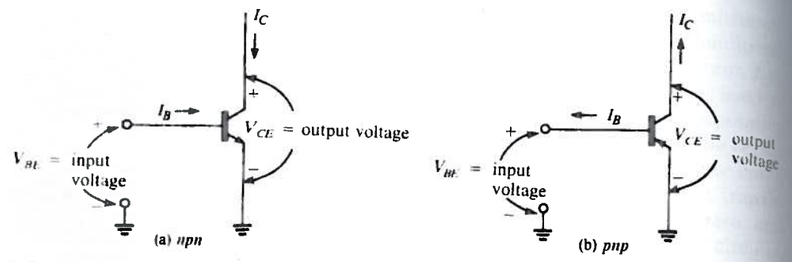


FIGURE 4–17 Input and output voltages and currents for *npn* and *pnp* transistors in the CE configuration

configuration is the most useful and most widely used transistor configuration, and we will study it in considerable detail. In the process we will learn some new facts about transistor behavior.

I_{CEO} and Beta

Before investigating the input and output characteristics of the CE configuration, we will derive a new relationship between I_C and I_{CBO}. Although this derivation does not depend in any way on the bias arrangement used, it will provide us with some new parameters that are useful for predicting leakage in the CE configuration and for relating CE input and output currents. Equation 4–2 states that

$$I_C = \alpha I_E + I_{CBO}$$

or

$$I_C - I_{CBO} = \alpha I_E$$

Dividing through by α,

$$\frac{I_C}{\alpha} - \frac{I_{CBO}}{\alpha} = I_E$$

Substituting $I_B + I_C$ for I_E on the right-hand side,

$$\frac{I_C}{\alpha} - \frac{I_{CBO}}{\alpha} = I_B + I_C$$

Collecting the terms involving I_C leads to

$$I_C\left(\frac{1}{\alpha} - 1\right) = I_B + \frac{I_{CBO}}{\alpha}$$

But $1/\alpha - 1 = (1 - \alpha)/\alpha$, so

$$I_C = \frac{\alpha I_B}{1 - \alpha} + \frac{I_{CBO}}{1 - \alpha} \tag{4–6}$$

Using equation 4–6, we can obtain an expression for reverse "leakage" current in the CE configuration. Figure 4–18 shows *npn* and *pnp* transistors in which the base–emitter circuits are left open while the reverse-biasing voltage sources remain connected. As can be seen in Figure 4–18, the only current that can flow when the base is left open is reverse current across the collector–base junction. This current flows from the collector, through the base region, and into the emitter. It is designated I_{CEO}—Collector-to-*E*mitter

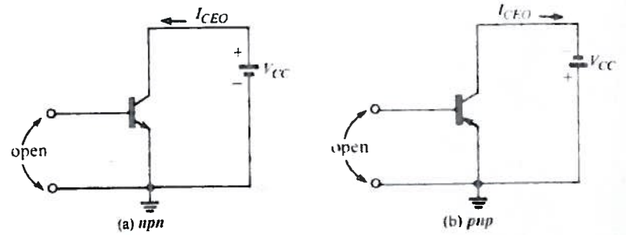


FIGURE 4–18 Collector–emitter leakage current I_{CEO}

current with the base *O*pen. (Note, once again, that this "reverse" current is in the same direction as normal collector current through the transistor.) Because I_B must equal 0 when the base is open, we can substitute $I_B = 0$ in equation 4–6 to obtain

$$I_{CEO} = \frac{I_{CBO}}{1 - \alpha} = \left(\frac{1}{1 - \alpha}\right) I_{CBO} \tag{4–7}$$

Because the α of a transistor is close to 1, $1 - \alpha$ is close to 0, and so $1/(1 - \alpha)$ can be quite large. Therefore, equation 4–7 tells us that CE leakage current is much larger than CB leakage current. For example, if $I_{CBO} = 0.1\ \mu A$ and $\alpha = 0.995$, then $I_{CEO} = (0.1\ \mu A)/0.005 = 20\ \mu A$. In effect, collector–base leakage current is amplified in the CE configuration, a result that can cause problems in high-temperature circuits, particularly those containing germanium transistors.

Returning to equation 4–6, let us focus on the factor $\alpha/(1 - \alpha)$ that multiplies I_B. This quantity is another important transistor parameter, called *beta:*

$$\beta = \frac{\alpha}{1 - \alpha} \tag{4–8}$$

Beta is always greater than 1 and for typical transistors ranges from around 20 to several hundred. When α is close to 1, a small increase in α causes a large increase in the value of β. For example, if $\alpha = 0.99$, then $\beta = 0.99/(1 - 0.99) = 99$. If α is increased by 0.005 to 0.995, then $\beta = 0.995/(1 - 0.995) = 199$. Because a small change in α causes a large change in β, small manufacturing variations in transistors that are supposed to be of the same type cause them to have a wide range of β values. It is not unusual for transistors of the same type to have betas that vary from 50 to 200.

In terms of β, equation 4–6 becomes

$$I_C = \beta I_B + \frac{I_{CBO}}{1 - \alpha} = \beta I_B + (\beta + 1) I_{CBO} \tag{4–9}$$

or

$$I_C = \beta I_B + I_{CEO} \tag{4–10}$$

Although I_{CEO} is much greater than I_{CBO}, it is generally quite small in comparison to βI_B, especially in silicon transistors, and it can be neglected in many practical circuits. Neglecting I_{CEO} in equation 4–10, we obtain the approximation $I_C \approx \beta I_B$. This approximation is widely used in transistor circuit analysis, and we will often write it as an equality in future discussions, with the understanding that I_{CEO} can be neglected:

$$I_C = \beta I_B \ (I_{CEO} = 0) \tag{4–11}$$

EXAMPLE 4–4

A transistor has $I_{CBO} = 48$ nA and $\alpha = 0.992$.

1. Find β and I_{CEO}.
2. Find its (exact) collector current when $I_B = 30$ μA.
3. Find the approximate collector current, neglecting leakage current.

Solution

1. $\beta = \dfrac{\alpha}{1-\alpha} = \dfrac{0.992}{0.008} = 124$

$I_{CEO} = \dfrac{I_{CBO}}{1-\alpha} = \dfrac{48 \times 10^{-9}}{0.008} = 6\ \mu A$ or $I_{CEO} = (\beta + 1)I_{CBO} = 6\ \mu A$

2. $I_C = \beta I_B + I_{CEO} = (124)(30\ \mu A) + 6\ \mu A = 3726\ \mu A = 3.726$ mA
3. $I_C \approx \beta I_B = 124(30\ \mu A) = 3.72$ mA

Equation 4–8 tells us how to find the β of a transistor, given its α. It is left as an exercise at the end of this chapter to show that we can find α, given β, by using the following relation:

$$\alpha = \frac{\beta}{\beta + 1} \tag{4–12}$$

EXAMPLE 4–5

As we will learn in a later discussion, the β of a transistor typically increases dramatically with temperature. If a certain transistor has $\beta = 100$ and an increase in temperature causes β to increase by 100%, what is the percent change in α?

Solution

A 100% increase in β means that β increases from 100 to 200. Let α_1 = value of α when $\beta = 100$ and α_2 = value of α when $\beta = 200$. From equation 4–12,

$$\alpha_1 = \frac{100}{100 + 1} = 0.990099$$

$$\alpha_2 = \frac{200}{200 + 1} = 0.995025$$

Thus, the percent change (increase) in α is

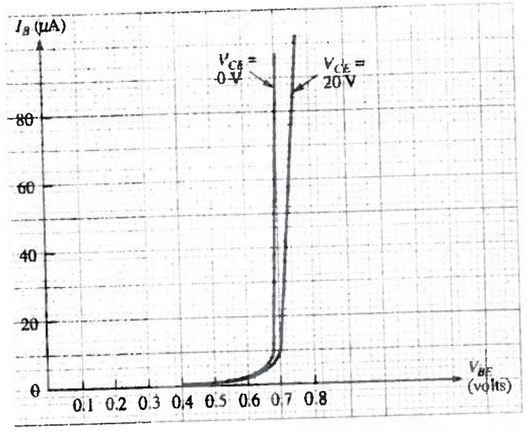
$$\frac{\alpha_2 - \alpha_1}{\alpha_1} \times 100\% = \frac{0.995025 - 0.990099}{0.990099} \times 100\% = 0.488\%$$

We see that a large change in β (100%) corresponds to a small change in α (0.488%).

Common-Emitter Input Characteristics

Because the input to a transistor in the CE configuration is across the base-to-emitter junction (see Figure 4–17), the CE input characteristics resemble a family of forward-biased diode curves. A typical set of CE input characteristics for an *npn* transistor is shown in Figure 4–19. Note that I_B increases as V_{CE} decreases, for a fixed value of V_{BE}. A large value of V_{CE} results in a large reverse bias of the collector–base junction, which widens the depletion region and makes the base smaller. When the base is smaller, there are fewer recombinations of injected minority carriers and there is a corresponding

FIGURE 4–19 Common-emitter input characteristics



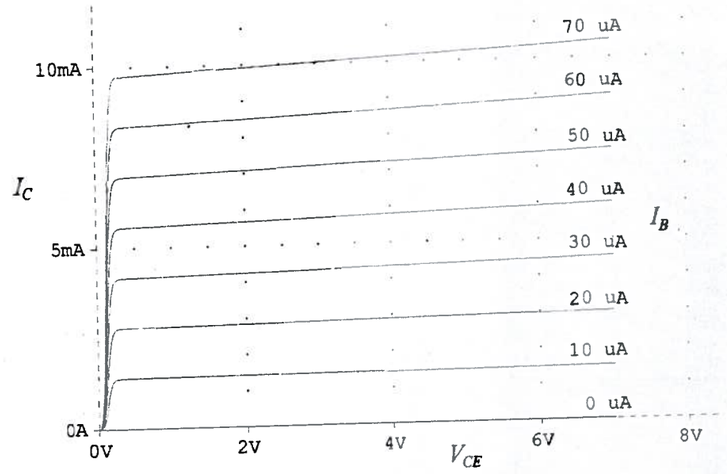


FIGURE 4–20 Common-emitter output characteristics

reduction in base current. In contrast to the CB input characteristics, note in Figure 4–19 that the input current is plotted in units of *micro*amperes. I_B is, of course, much smaller than either I_E or I_C ($I_B \approx I_C/\beta$). The CE input characteristics are often called the *base characteristics*.

Common-Emitter Output Characteristics

Common-emitter output characteristics show collector current I_C versus collector voltage V_{CE}, for different *fixed* values of I_B. These characteristics are often called *collector characteristics*. Figure 4–20 shows a typical set of output characteristics for an *npn* transistor in the CE configuration.

The approximate value of the β of the transistor can be determined at any point on the characteristic in Figure 4–20 simply by dividing the values I_C/I_B at the point. As illustrated in the figure, at $V_{CE} = 3$ V and $I_B = 50$ μA, the value of I_C is about 7 mA, and the value of the β at that point is therefore I_C/I_B = (7 mA)/(50 μA) = 140. Clearly β, like α, is not constant, but depends on the

region of the characteristics where the transistor is operated. The region where the curves are approximately horizontal is the *active* region of the CE configuration. In this region, β is essentially constant but increases somewhat with V_{CE}, as can be deduced from the rise in each curve as V_{CE} increases to the right.

As in the CB configuration, the collector current in the CE configuration will increase rapidly if V_{CB} is permitted to become large. When $I_B = 0$ (base open), the collector-to-emitter current at which breakdown occurs is designated BV_{CEO}. The value of BV_{CEO} is always less than that of BV_{CBO} for a given transistor. BV_{CEO} is sometimes called the "sustaining voltage" and denoted LV_{CEO}.

When interpreting the characteristics of Figure 4–20, it is important to realize that each curve is drawn for a small, essentially constant value of V_{BE} (about 0.7 V for silicon). Figure 4–21 illustrates this point. Note in Figure 4–21 that the total collector-to-emitter voltage V_{CE} (which is the same as V_{CC} in our case) is the sum of the small, forward-biasing value of V_{BE} and the reverse-biasing value of V_{CB}. Thus $V_{CE} = V_{CB} + V_{BE}$, or, for silicon, $V_{CE} \approx V_{CB} + 0.7\text{V}$. Thus, if V_{CE} is reduced to about 0.7 V, V_{CB} must become 0, and the collector–base junction is no longer reverse biased. This effect can be seen in the characteristics of Figure 4–20. Notice that each curve is reasonably flat (in the active region) until V_{CE} is reduced to around 0.2 V to 0.3 V. As V_{CE} is reduced further, I_C starts to fall off. When V_{CE} is reduced below about 0.2 V or 0.3 V, the collector–base junction becomes well *forward* biased and collector current diminishes rapidly. Remember that V_{CB} is negative when the collector–base junction is forward biased. For example, if $V_{CE} = 0.2\text{ V}$, then $V_{CB} = V_{CE} - V_{BE} \approx 0.2\text{ V} - 0.7\text{ V} = -0.5\text{ V}$. In keeping with our previous definition, the transistor is said to be *saturated* when the collector–base junction is forward biased. The saturation region is shown on the characteristic curves. The saturation value of V_{CE}, designated $V_{CE(sat)}$, ranges from 0.1 V to 0.3 V, depending on the value of base current.

Notice in Figure 4–20 that when $I_B = 0$, the collector current is the same as that which flows when the base circuit is open (see Figure 4–18), that is, I_{CEO}. The region below $I_B = 0$ is the *cut-off* region.

Comparing the CB output characteristics in Figure 4–14 with the CE output characteristics in Figure 4–20, we note that the curves rise more steeply to the right in the CE case. This rise simply reflects the fact we have already discussed in connection with the CE input characteristics: The greater the value of V_{CE}, the smaller the base region and, consequently, the smaller the base current. But, because base current is constant along each curve in Figure 4–20, the effect appears as an increase in I_C. In other words, the fact that there are fewer recombinations occurring in the base means that a greater proportion of carriers cross the junction to become collector current.

It is apparent in Figure 4–20 that the characteristic curves corresponding to large values of I_B rise more rapidly to the right than those corresponding

FIGURE 4–21 $V_{CE} \approx V_{CB} + 0.7\text{ V}$ for silicon. When V_{CE} is reduced to about 0.7 V, then $V_{CB} \approx 0$ and the collector–base junction is no longer reverse biased

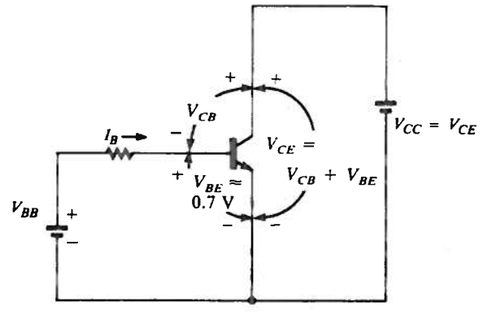
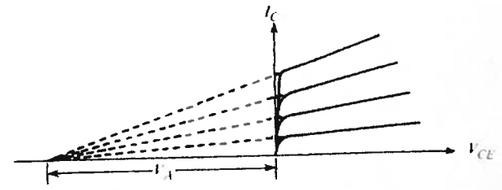


FIGURE 4–22 The Early voltage, V_A, is the intersection of the characteristic curves with the horizontal axis



to small values of I_B. If these lines are projected to the left, as shown in Figure 4–22, it is found that they all intersect the horizontal axis at approximately the same point. The point of intersection, designated V_A in Figure 4–22, is called the *Early voltage*, after J. M. Early, who first investigated these relations. Of course, a transistor is never operated with V_{CE} equal to the Early voltage. V_A is simply another useful parameter characterizing a transistor's behavior. It is especially useful in computer simulation programs such as SPICE that analyze transistor circuits and require complete descriptions of transistor characteristics.

EXAMPLE 4–6

A certain transistor has the output characteristics shown in Figure 4–20.

1. Find the percent change in β as V_{CE} is changed from 1 V to 4 V while I_B is fixed at 40 μA.
2. Find the percent change in β as I_B is changed from 10 μA to 50 μA while V_{CE} is fixed at 3.5 V.

Neglect leakage current in each case.

Solution

1. At the intersection of the vertical line $V_{CE} = 1\text{ V}$ with the curve $I_B = 40\ \mu\text{A}$, we find $I_C \approx 5.6$ mA. Therefore, the β at that point is approximately (5.6 mA)/(40 μA) = 140.

   Traveling along the curve of constant $I_B = 40\ \mu\text{A}$ to its intersection with the vertical line $V_{CE} = 4\text{V}$, we find $I_C \approx 7.2$ mA. Therefore, $\beta \approx (7.2\text{mA})/(40\ \mu\text{A}) = 180$. The percent change in β is

$$\frac{180 - 140}{140} \times 100\% = 28.57\%$$

2. At the intersection of the vertical line $V_{CE} = 3.5\text{ V}$ with the curve $I_B = 10\ \mu\text{A}$, we find $I_C \approx 1.4$ mA. Therefore, $\beta \approx (1.4\text{ mA})/(10\ \mu\text{A}) = 140$.

   Traveling up the vertical line of constant $V_{CE} = 3.5\text{ V}$ to its intersection with the curve $I_B = 50\ \mu\text{A}$, we find $I_C \approx 7.3$ mA. Therefore, $\beta \approx (7.3\text{ mA})/(50\ \mu\text{A}) = 146$. The percent change in β is

$$\frac{146 - 140}{140} \times 100\% = 4.28\%$$

EXAMPLE 4–7

SPICE

(Computer Generation of Characteristic Curves) Use SPICE to obtain a set of output characteristics for an *npn* transistor in a CE configuration. The ideal maximum forward β is 100 and the Early voltage is 100 V. The characteristics should be plotted for V_{CE} ranging from 0 V to 15.0 V in 0.05-V steps and for I_B ranging from 0 to 40 μA in 10-μA steps. Use the results to determine the actual value of β at $V_{CE} = 10\text{ V}$ and $I_B = 30\ \mu\text{A}$.

FIGURE 4–23(A) (Example 4–7)

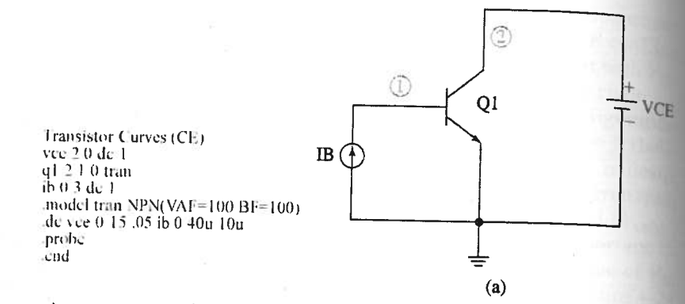
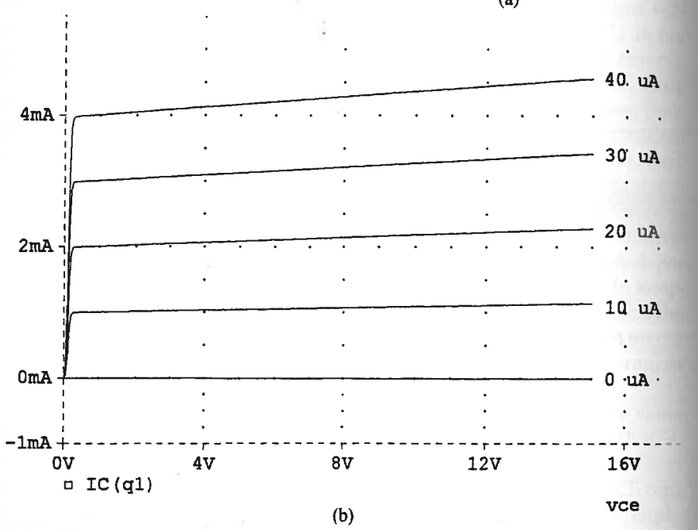


FIGURE 4–23(B) (Example 4–7)



Solution

Figure 4–23(a) shows the circuit and the SPICE input file. Note that a constant-current source is used to supply base current. The transistor .MODEL statement specifies that β = 100 (BF = 100) and that the (forward) Early voltage VAF = 100 V.

The .DC statement is the *dc sweep* command that causes V_{CE} to be stepped in .05-V increments from 0 to 15.0 V and I_B to be stepped in 10-μA increments from 0 to 40 μA. The plot generated by the SPICE analysis and the Probe option is shown in Figure 4–23(b). Notice that at V_{CE} = 15.0 V and I_B = 20 μA, it can be seen from the graphical plot that I_C = 2.3 mA. Thus,

$$\beta = \frac{I_C}{I_B} = \frac{2.3\text{ mA}}{20\ \mu\text{A}} = 115$$

Note how the slope of the curves increase for an increasing voltage value of V_{CE}. This is due to the effect of the Early voltage, meaning that β increases with increasing V_{CE} (and with increasing I_B).

4–5 COMMON-COLLECTOR CHARACTERISTICS

In the third and final way to arrange the biasing of a transistor, the collector is made the common point. The result is called the *common-collector* (CC) configuration and is illustrated in Figure 4–24. It is apparent in Figure 4–24(a) that

$$V_{CE} = V_{CB} + V_{BE} \tag{4–13}$$

or $V_{CB} = V_{CE} - V_{BE}$. In our case, $V_{CE} = V_{CC}$ and $V_{CB} = V_{BB}$, so $V_{BB} = V_{CC} - V_{BE}$. Now V_{BE} is the small, essentially constant voltage across the forward-biased base-to-emitter junction (about 0.7 V for silicon). Thus,

$$V_{BB} = V_{CB} \approx V_{CC} - 0.7\text{ V} \tag{4–14}$$

Therefore, in order to keep the collector–base junction reverse biased ($V_{CB} > 0$), it is necessary that V_{BB} be larger than V_{CC} − 0.7 V.

Figure 4–25 shows that the base–collector voltage is the input voltage and the base current is the input current. The emitter–collector voltage is the output voltage, and the emitter current is the output current.

Figure 4–26 shows a typical set of input characteristics for an *npn* transistor in the CC configuration. It is clear that these are not the characteristics of a forward-biased diode, as they were in the CB and CE configurations. We can see that each curve is drawn for a different fixed value of V_{CE} and that each shows the base current going to 0 very quickly as V_{CB} increases slightly. This behavior can be explained by remembering that V_{BE} must remain in the neighborhood of 0.5 V to 0.7 V in order for any appreciable base current to flow. But, from equation 4–13,

$$V_{BE} = V_{CE} - V_{CB} \tag{4–15}$$

FIGURE 4–24 The common-collector (*CC*) bias configuration

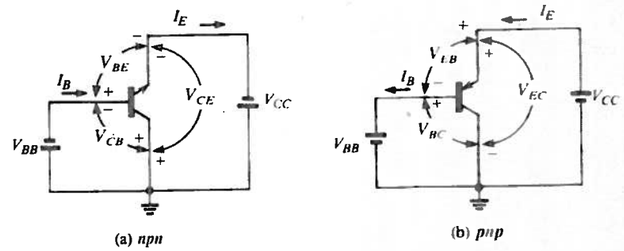


FIGURE 4–25 Input and output voltages and currents in the CC configuration

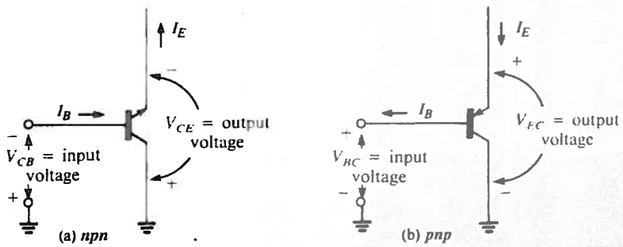
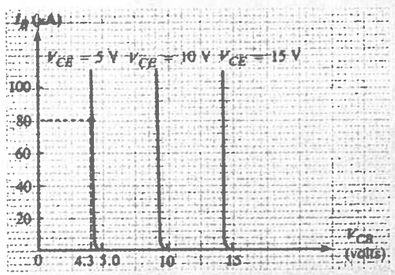


FIGURE 4–26 Common-collector input characteristics



Therefore, if the value of V_{CB} is allowed to increase to a point where it is near the value of V_{CE}, the value of V_{BE} approaches 0, and no base current will flow. In Figure 4–26, refer to the curve that corresponds to $V_{CE} = 5$ V. When $V_{CB} = 4.3$ V, we have, from equation 4–15, $V_{BE} = 5 - 4.3 = 0.7$ V, and we therefore expect a substantial base current. In the figure, we see that the point $V_{CB} = 4.3$ V and $V_{CE} = 5$ V yields a base current of 80 μA. If V_{CB} is now allowed to increase to 5 V, then $V_{BE} = 5 - 5 = 0$ V, and the base–emitter junction is no longer forward biased. Note in the figure that $I_B = 0$ when $V_{CE} = V_{CB} = 5$ V.

Figure 4–27 shows a typical set of CC output characteristics for an *npn* transistor. These show emitter current, I_E, versus collector-to-emitter voltage, V_{CE}, for different fixed values of I_B. Note that these curves closely resemble the CE output characteristics shown in Figure 4–20. This resemblance is expected, because the only distinction is that I_E in Figure 4–27 is along the vertical axis instead of I_C, and $I_E \approx I_C$.

When leakage current is neglected, recall that $I_C = \beta I_B$. But $I_E = I_C + I_B = \beta I_B + I_B$. Therefore,

$$I_E = (\beta + 1)I_B \tag{4–16}$$

Equation 4–16 relates the input and output currents in the CC configuration.

4–6 BIAS CIRCUITS

In our discussion of BJT theory up to this point, we have been using the word *bias* simply to specify the polarity of the voltage applied across each of the *pn* junctions in a transistor. In that context, we have emphasized that the base–emitter junction must be forward biased and the collector–base junction must be reverse biased to achieve normal transistor action. We wish now

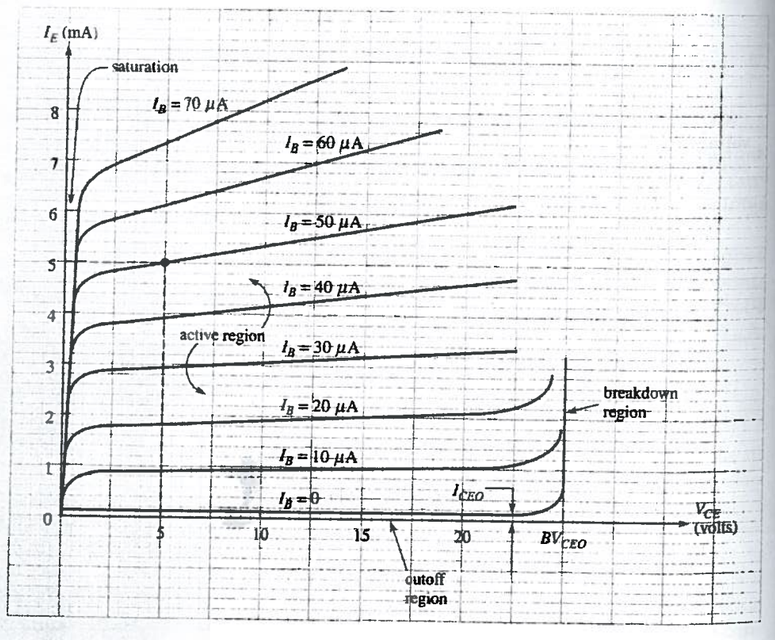


FIGURE 4–27 Common-collector output characteristics

to adopt a more restrictive interpretation of "bias." Henceforth, we will be concerned with adjusting the *value* of the bias, as needed, to obtain *specific* values of input and output currents and voltages. In other words, we accept the fact that both junctions must be biased in the proper *direction* and concentrate on a practical means for changing the *degree* of bias so that the output voltage, for example, is exactly the value we want it to be. When we have achieved a specific output voltage and output current, we say that we have set the *bias point* to those values.

Common-Base Bias Circuit

In practical circuits, we control the bias by connecting external resistors in series with the external voltage sources V_{CC}, V_{EE}, etc. We can then change resistor values instead of voltage source values to control the dc input and output voltages and currents. The circuit used to set the bias point this way is called a *bias circuit*. Figure 4–28 shows common-base bias circuits in which a resistor, R_E, is connected in series with the emitter and a resistor, R_C, is in series with the collector. Notice that we still regard emitter current as input current and base–emitter voltage as input voltage as in past discussions of the CB configuration (see Figure 4–10). Likewise, collector current and collector–base voltage are still outputs. The only difference is that the input voltage is no longer the same as V_{EE} because there is a voltage drop across R_E, and the output voltage is no longer the same as V_{CC} due to the drop across R_C. The external voltage sources V_{EE} and V_{CC} are called *supply* voltages. Of course, the characteristic curves are still perfectly valid for showing the relationships between input and output voltages and currents.

Writing Kirchhoff's voltage law around the collector–base loop in Figure 4–28(a), we have

$$V_{CC} = I_C R_C + V_{CB} \tag{4–17}$$

Rearranging equation 4–17 leads to

$$I_C = \frac{-1}{R_C} V_{CB} + \frac{V_{CC}}{R_C} \tag{4–18}$$

When we regard I_C and V_{CB} as variables and V_{CC} and R_C as constants, we see that equation 4–18 is the equation of a straight line. When plotted on a set of I_C–V_{CB} axes, the line has slope $-1/R_C$, and it intercepts the I_C-axis at V_{CC}/R_C. Equation 4–18 is the equation for the (*npn*) CB *load line*. This load line has exactly the same interpretation as the diode load line we studied in Chapter 3: It is the line through *all possible* combinations of voltage (V_{CB}) and current (I_C). The actual bias point must be a point lying somewhere on the line. The precise location of the point is determined by the input current I_E.

We can find the point where the load line intercepts the V_{CB}-axis by setting $I_C = 0$ in equation 4–18 and solving for V_{CB}. Do this as an exercise and verify that the V_{CB}-intercept is $V_{CB} = V_{CC}$. Thus, the load line can be drawn simply by drawing a line through the two points $V_{CB} = 0$, $I_C = V_{CC}/R_C$ and $I_C = 0$, $V_{CB} = V_{CC}$.

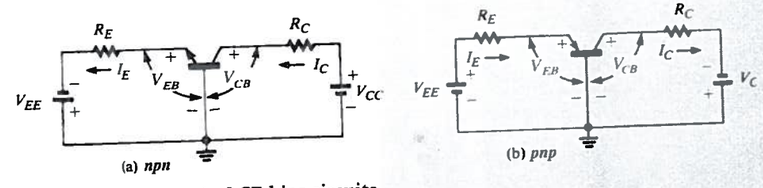


FIGURE 4–28 Practical CB bias circuits

FIGURE 4–29 (Example 4–8)

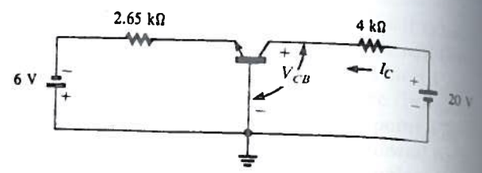
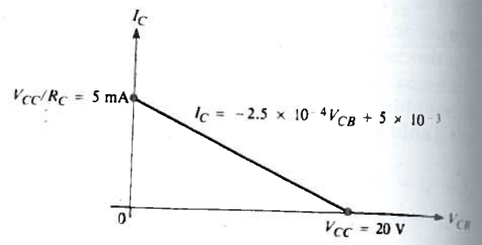


FIGURE 4–30 (Example 4–8) Load line for the bias circuit shown in Figure 4–29



EXAMPLE 4–8

Determine the equation of the load line for the circuit shown in Figure 4–29. Sketch the line.

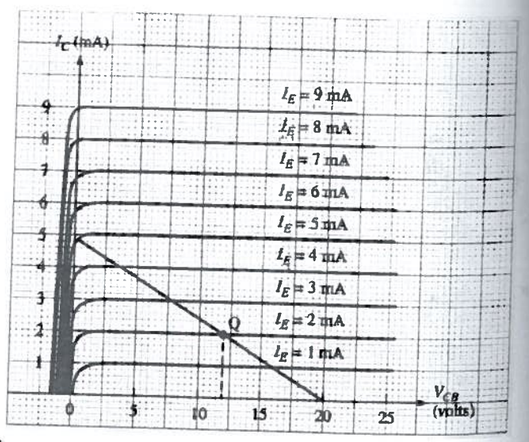
Solution

$$I_C = \frac{-1}{R_C} V_{CB} + \frac{V_{CC}}{R_C}$$
$$= \frac{-1}{4 \times 10^3} V_{CB} + \frac{20}{4 \times 10^3}$$
$$= -2.5 \times 10^{-4} V_{CB} + 5 \times 10^{-3} \text{A}$$

The load line has slope -2.5×10^{-4} S, intercepts the I_C-axis at 5 mA, and intercepts the V_{CB}-axis at 20 V. It is sketched in Figure 4–30.

We can determine the bias point by plotting the load line on the output characteristics of the transistor used in the circuit. To illustrate, the load line determined in Example 4–8 is shown drawn on a set of CB output characteristics in Figure 4–31.

FIGURE 4–31 Load line plotted on CB output characteristics. The bias point (or quiescent point, labeled Q) is the intersection of the load line with the I_E = 2 mA curve.



To locate the bias point on the load line shown in Figure 4–31, we must determine the emitter current I_E in the circuit of Figure 4–29. One way to find I_E would be to draw an *input* load line on an input characteristic and determine the value of I_E where the line intersects the characteristic. This is the same technique used in Chapter 3 to find the dc current and voltage across a forward-biased diode in series with a resistor, which is precisely what the input side of the transistor circuit is. However, this approach is not practical for several reasons, not the least of which is the fact that input characteristics are seldom available.

The most practical way to determine I_E is to regard the base–emitter junction as a forward-biased diode having a fixed drop of 0.7 V (silicon) and solve for the diode current, the way we did in Chapter 3. Refer to Figure 4–32. In Figure 4–32, it is evident that

$$I_E = \frac{V_{EE} - 0.7}{R_E} \tag{4–19}$$

Note that we are neglecting the "feedback" effect of V_{CB} on the emitter current. Also note that the positive side of V_{EE} is connected to the circuit common, or ground, so it would normally be referred to as a *negative* voltage with respect to ground. However, in our equations, we treat V_{EE} as the absolute value of that voltage. Returning to our example circuit of Figure 4–29, we apply equation 4–19 to find

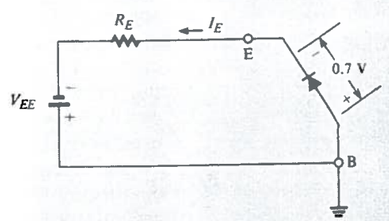
$$I_E = \frac{(6 - 0.7)\text{ V}}{2.65\text{ k}\Omega} = 2\text{ mA}$$

In Figure 4–31, the bias point, labeled Q, is seen to be the intersection of the load line with the curve I_E = 2 mA. At that point, $I_C \approx 2$ mA and V_{CB} = 12 V.

The bias point is often called the *quiescent* point, *Q*-point, or *operating* point. It specifies the dc output voltage and current when no ac voltage is superimposed on the input. As we shall discover in Chapter 7, the circuit is used as an *ac amplifier* by connecting an ac voltage source in series with the emitter. As the ac voltage alternately increases and decreases, the emitter current does the same. As a result, the output voltage and current change *along the load line* over a range determined by the change in I_E values.

Transistor input and output characteristics are useful for gaining insights into transistor behavior, and, when used with load lines, they help us visualize output current and voltage variations. However, they are seldom used to design or analyze transistor circuits. One reason they are not is that transistors of the same type typically have a wide variation in their characteristics. For that reason, manufacturers do not (cannot) publish a set of curves that could be used for every transistor of a certain type. Furthermore, the accuracy that can be obtained using approximations and purely algebraic methods of analysis (as opposed to graphical methods) is almost always adequate for practical applications. We have already seen an example of this

FIGURE 4–32 The input side of the transistor in a CB configuration can be regarded as a forward-biased diode for purposes of calculating I_E.



kind of algebraic approximation, when we regarded the input to the CB transistor as a forward-biased diode having a fixed voltage drop. We will now show how the entire bias circuit can be analyzed without the use of characteristic curves.

Because $\alpha \approx 1$ and $I_C = \alpha I_E$, it is true that $I_C \approx I_E$. Therefore, once we have determined I_E using equation 4–19, $I_E = (V_{EE} - 0.7)/R_E$ (silicon), we have a good approximation for I_C. We can then use equation 4–17 to solve for V_{CB}:

$$V_{CB} = V_{CC} - I_C R_C \tag{4–20}$$

EXAMPLE 4–9

Determine the bias point of the circuit shown in Figure 4–29 without using characteristic curves.

Solution

We have already shown (equation 4–19) that

$$I_E = \frac{V_{EE} - 0.7}{R_E} = \frac{(6 - 0.7)\text{ V}}{2.65\text{ k}\Omega} = 2\text{ mA}$$

Then, using $I_C \approx I_E$, we have from equation 4–20

$$\begin{aligned} V_{CB} &= V_{CC} - I_C R_C \\ &= 20\text{ V} - (2 \times 10^{-3}\text{ A})(4 \times 10^3\ \Omega) = 20\text{ V} - 8\text{ V} = 12\text{ V} \end{aligned}$$

Note that the bias point computed this way, $I_C = 2$ mA and $V_{CB} = 12$ V, is the same as that found graphically in Figure 4–31.

Summarizing, here are the four equations that can be used to solve for all input and output currents and voltages in the *npn* CB bias circuit of Figure 4–28(a):

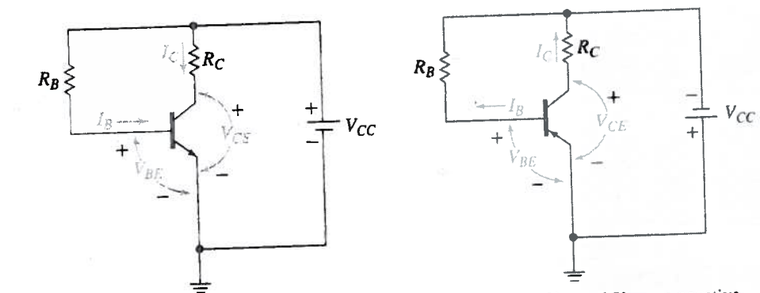
$$\boxed{\begin{aligned} V_{BE} &= 0.7\text{ V (Si)},\quad 0.3\text{ V (Ge)} \\ I_E &= \frac{V_{EE} - V_{EB}}{R_E} \\ I_C &\approx I_E \\ V_{CB} &= V_{CC} - I_C R_C \end{aligned}} \tag{4–21}$$

Equations 4–21 can be used for *pnp* transistors (Figure 4–28(b)) by substituting absolute values for V_{EB}, V_{CB}, and V_{CC}. For example, if we have $I_C = 1$ mA, $R_C = 1$ kΩ, and $V_{CC} = -15$ V in the *pnp* circuit of Figure 4–28(b), then $|V_{CB}| = 15 - (1\text{ mA})(1\text{ k}\Omega) = 5$ V. Since the base terminal is common in this circuit, the output voltage is expressed with the base as reference, i.e., as V_{CB}. Of course, $V_{CB} = -5$ V in this example.

Common-Emitter Bias Circuit

Figure 4–33 shows practical bias circuits for *npn* and *pnp* transistors in the common-emitter configuration. Notice that these bias circuits use only a single supply voltage (V_{CC}), which is a distinct practical advantage. The values of R_B and R_C must be chosen so that the voltage drop across R_B is greater than the voltage drop across R_C in order to keep the collector–base junction reverse biased. The selection of values for R_B and R_C is part of the procedure used to design a CE bias circuit, which we will cover in Chapter 7.

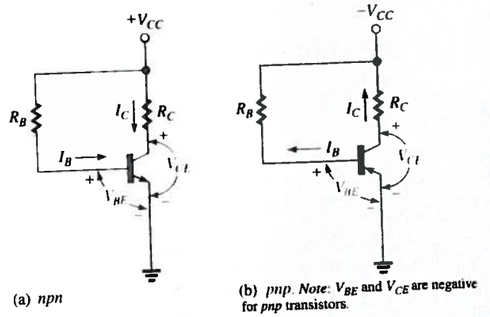
As discussed in Chapter 3, it is important to be able to visualize the operation of electronic circuits when their diagrams are drawn without the ground paths shown because that is the usual practice. The schematic



(a) *npn* (b) *pnp*. *Note*: V_{BE} and V_{CE} are negative for *pnp* transistors.

FIGURE 4–33 Practical CE bias circuits. *Note*: V_{BE} and V_{CE} are negative for *pnp* transistors

FIGURE 4–34 Schematic diagrams of the CE bias circuits shown in Figure 4–33, with ground paths omitted



(a) *npn* (b) *pnp*. *Note*: V_{BE} and V_{CE} are negative for *pnp* transistors.

diagrams in Figure 4–33 are useful for identifying closed loops, around which Kirchhoff's voltage law can be written, but the diagrams are rarely drawn as shown. Figure 4–34 shows the conventional way of drawing schematic diagrams of the CE bias circuits. As we have done in Figure 4–34, we will hereafter omit the ground paths in transistor schematics. When studying an example or working an exercise, feel free to draw in any omitted ground paths whose presence would aid in understanding the circuit.

By writing Kirchhoff's voltage law around the output loop in Figure 4–33(a) or 4–34(a), we can obtain the equation for the load line of an *npn* transistor in a CE configuration: $V_{CC} = I_C R_C + V_{CE}$, or

$$I_C = \frac{-1}{R_C} V_{CE} + \frac{V_{CC}}{R_C} \tag{4–22}$$

Note the similarity of equation 4–22 to the equation for the CB load line (4–18). The CE load line has slope $-1/R_C$, intercepts the I_C-axis at V_{CC}/R_C, and intercepts the V_{CE}-axis at V_{CC}. Figure 4–35 shows a graph of the load line plotted on I_C–V_{CE}-axes.

When the CE load line is plotted on a set of CE output characteristics, the bias point can be determined graphically, provided the value of I_B is known. To determine the value of I_B, we can again regard the input side of the transistor as a forward-biased diode having a fixed voltage drop, as shown in Figure 4–36. From Figure 4–36, we see that

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \tag{4–23}$$

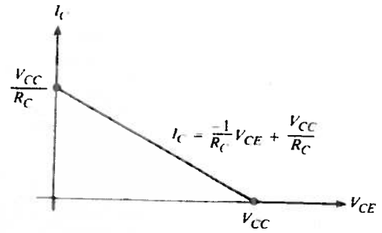


FIGURE 4–35 The CE load line for the bias circuit in Figure 4–34(a)

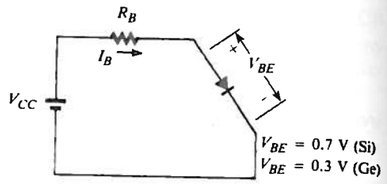


FIGURE 4–36 The input to an *npn* transistor in the CE configuration can be regarded as a forward-biased diode having a fixed voltage drop

where V_{BE} = 0.7 V for silicon and 0.3 V for germanium. Once again, we neglect the feedback effect of V_{CE} on I_B (the effect shown in Figure 4–19). As in the case of the CB bias circuit, the CE bias point can be determined algebraically. The equations for an *npn* circuit are summarized as follows:

$$\begin{aligned} V_{BE} &= 0.7\text{ V (Si)},\ 0.3\text{ V (Ge)} \\ I_B &= \frac{V_{CC} - V_{BE}}{R_B} \\ I_C &= \beta I_B \\ V_{CE} &= V_{CC} - I_C R_C \end{aligned} \tag{4–24}$$

Equations 4–24 can be applied to a *pnp* bias circuit (Figure 4–34(b)) as demonstrated in Example 4–10(b).

EXAMPLE 4–10

a. The silicon transistor in the CE bias circuit shown in Figure 4–37(a) has a β of 100.

1. Assuming that the transistor has the output characteristics shown in Figure 4–38, determine the bias point graphically.
2. Find the bias point algebraically.
3. Repeat (1) and (2) when R_B is changed to 161.43 kΩ.

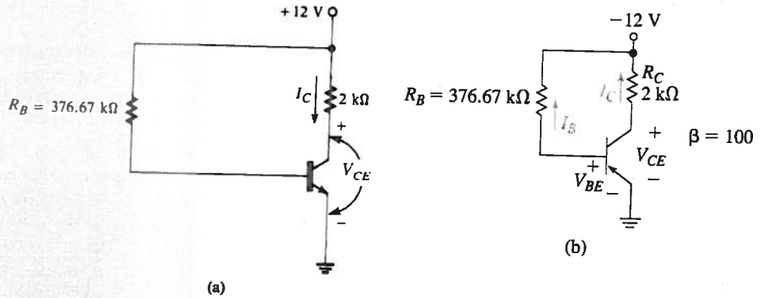
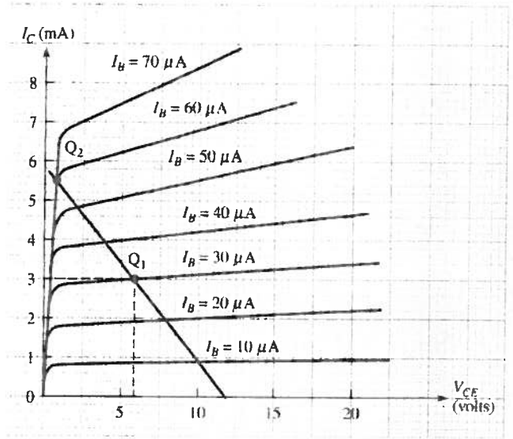


FIGURE 4–37 (Example 4–10)

FIGURE 4–38 Load line plotted on CE output characteristics (Example 4–10). The bias point is shifted (into saturation) by the change in R_B.



Solution

1. The equation of the load line is

$$\begin{aligned} I_C &= -\frac{1}{2 \times 10^3}V_{CE} + \frac{12}{2 \times 10^3} \\ &= -0.5 \times 10^{-3}V_{CE} + 6 \times 10^{-3} \end{aligned}$$

The load line intersects the I_C-axis at 6 mA and the V_{CE}-axis at 12 V. It is shown plotted on the output characteristics in Figure 4–38. To locate the bias point, we find I_B:

$$I_B = \frac{(12 - 0.7)\text{ V}}{376.67\text{ k}\Omega} = 30\ \mu\text{A}$$

At the intersection of the I_B = 30 μA curve with the load line, labeled Q_1 in Figure 4–38, we see that the bias point is $I_C \approx 2.95$ mA and V_{CE} = 6 V.

2. From equations 4–24, we find

$$V_{BE} = 0.7\text{ V}$$

$$I_B = \frac{(12 - 0.7)\text{ V}}{376.67\text{ k}\Omega} = 30\ \mu\text{A}$$

$$I_C = (100)(30\ \mu\text{A}) = 3\text{ mA}$$

$$V_{CE} = 12\text{ V} - (3\text{ mA})(2\text{ k}\Omega) = 6\text{ V}$$

These results are in good agreement with the bias values found graphically.

3. Changing R_B to 161.43 kΩ has no effect on the load line. Note that the load line equation (4–22) does not involve R_B. However, the value of I_B is changed to

$$I_B = \frac{(12 - 0.7)\text{ V}}{161.43\text{ k}\Omega} = 70\ \mu\text{A}$$

Thus, the bias point is shifted along the load line to the point labeled Q_2 in Figure 4–38. We see that Q_2 is now in the saturation region of the transistor. At Q_2, $I_C \approx 5.7$ mA and $V_{CE} \approx 0.5$ V. This result illustrates that the bias point can be changed by changing the value of external resistor(s) in the bias circuit.

Using equations 4–24 to find the new bias point, we have

$$I_C = \beta I_B = (100)(70\ \mu A) = 7\ mA \quad (!)$$

$$V_{CE} = 12\ V - (7\ mA)(2\ k\Omega) = -2\ V \quad (!)$$

These are clearly erroneous results because the maximum value that I_C can have is 6 mA, and the minimum value that V_{CE} can have is 0 V. The reason equations 4–24 are not valid in this case is that the bias point is not in the active region. Remember that β decreases in the saturation region, and, in this example, can no longer be assumed to equal 100. (As an exercise, use Figure 4–38 to calculate the value of β at Q_2.)

b. For the *pnp* silicon transistor circuit shown in Figure 4–37(b), determine the following (assume β = 100):

1. Find the base current I_B.
2. Find the collector current I_C.
3. Find V_{CE}.

Solution

First examine Figure 4–37(b). Note that the currents and polarities of all voltages are indicated. V_{CE} and V_{BE} look the same as an *npn*. It is not necessary to write V_{CE} as V_{EC} and V_{BE} as V_{EB}. For a properly biased *pnp* circuit, these voltages will be negative (base–emitter junction forward biased and collector–base junction reverse biased).

1. To solve for I_B, write the KVL equation as follows:

$$-V_{CC} + I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} + V_{BE}}{R_B}$$

$$= \frac{12.0 - 0.7}{376.67\ k\Omega} = 30\ \mu A$$

2. To solve for I_C, use the equation

$$I_C = \beta I_B = 100 \times 30\ \mu A = 3\ mA$$

3. To solve for V_{CE}, write the KVL equation as follows:

$$-V_{CC} + I_C R_C - V_{CE} = 0 \rightarrow V_{CE} = -V_{CC} + I_C R_C$$
$$V_{CE} = -12.0 + (3\ mA)(2\ k\Omega)$$
$$V_{CE} = -6\ V$$

Note: V_{CE} is a negative value as expected. Also note that I_B and V_{CE} have the same magnitude values as the *npn* circuit. This technique makes the analysis of *npn* and *pnp* circuits almost identical.

EXAMPLE 4–11

Use SPICE analysis to find the bias points of the CE circuit shown in Figure 4–37.

Solution

The circuit is redrawn with the nodes for the SPICE analysis as shown in Figure 4–39. Ground is always listed as node 0 (zero). The listing for the .CIR file follows. The .DC command specifies that the simulation will step the VCC

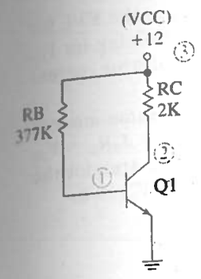


FIGURE 4–39 The CE circuit used in the simulation for Example 4–11

voltage from 0.0 V to 12.0 V in 0.1-V increments. The .OP command is used to tell the SPICE simulation to calculate the operating point values. This value is available in the output (.out) file.

```
Example 4-11
VCC 3 0 DC 12.0
Q1 2 1 0 NTRAN
RB 3 1 377k
RC 3 2 2k
.MODEL NTRAN NPN BF=100
.OP
.END
```

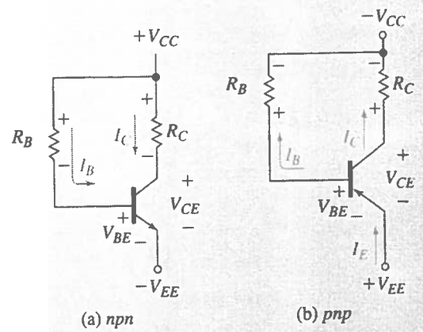
The following information was obtained by "Browsing" the output file (.out). Only a portion of the output file is listed.

```
**** SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 27.000 DEG C
NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE
(1) .8024 (2) 6.0596 (3) 12.0000
VOLTAGE SOURCE CURRENTS
NAME CURRENT
VCC -3.000E-03
OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C
BIPOLAR JUNCTION TRANSISTORS
NAME Q1
MODEL NTRAN
IB 2.97E-05
IC 2.97E-03
VBE 8.02E-01
VBC -5.26E+00
VCE 6.06E+00
```

The SPICE simulation results show that I_B = 29.7 μA, I_C = 2.97 mA, and V_{CE} = 6.0596 V. These values are in close agreement with the results obtained in Example 4–10.

The examples presented for common-emitter circuits use only a $+V_{CC}$ and ground connections. In some cases, it is desirable to power the circuit using a dual power supply (i.e., $+V_{CC}$ and $-V_{EE}$). Examples of these circuits are shown in Figures 4–40(a) and (b) for *npn* and *pnp* circuits. Analysis of these circuits is possible by writing KVL equations along input and output paths.

FIGURE 4–40 Common-emitter circuits using dual power supplies



For the *npn* circuit in 4–40(a), I_B can be obtained by writing the KVL for the base current loop as follows: $V_{CC} - I_B R_B - V_{BE} + V_{EE} = 0$. Solving for V_{CE} requires that the KVL equation be written for the collector–emitter current loop as follows: $V_{CC} - I_C R_C - V_{CE} + V_{EE} = 0$.

For the *pnp* circuit in 4–40(b), I_B can be calculated in the same manner by writing the KVL for the base current loop as follows: $-V_{CC} + I_B R_B - V_{BE} - V_{EE} = 0$. Solving for V_{CE} requires that the KVL equation be written for the collector–emitter current loop as follows: $-V_{CC} + I_C R_C - V_{CE} - V_{EE} = 0$.

Common-Collector Bias Circuit

Figure 4–41 shows common-collector bias circuits for *npn* and *pnp* transistors. Once again, the load line for Figure 4–41(a) can be derived by writing Kirchhoff's voltage law around the output loop:

$$V_{CC} = I_E R_E + V_{CE}$$

$$I_E = \frac{-1}{R_E} V_{CE} + \frac{V_{CC}}{R_E} \qquad (4\text{–}25)$$

Recall that the output characteristics for the CC configuration are, for all practical purposes, the same as those for the CE configuration. Therefore, we will not present another example showing the load line plotted on output characteristics.

As in the previous configurations, we must find I_B in order to determine the bias point. Figure 4–42 shows a circuit that is equivalent to the loop in Figure 4–41(a) that starts at V_{CC}, passes through R_B, through the base–emitter junction, through R_E, and back to V_{CC}. Writing Kirchhoff's voltage law around the loop in Figure 4–42, we have

$$V_{CC} = I_B R_B + V_{BE} + I_E R_E \qquad (4\text{–}26)$$

By equation 4–16, $I_E = (\beta + 1) I_B$. Substituting for I_E in equation 4–26, we obtain

$$V_{CC} = I_B R_B + V_{BE} + (\beta + 1) I_B R_E$$

or

$$V_{CC} - V_{BE} = I_B [R_B + (\beta + 1) R_E]$$

Solving for I_B,

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E} \qquad (4\text{–}27)$$

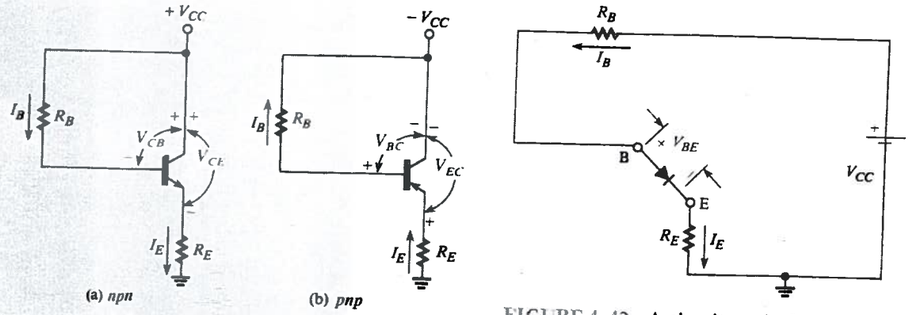


FIGURE 4–41 Common-collector bias circuits

FIGURE 4–42 A circuit equivalent to the input side of Figure 4–41(a)

Summarizing, the equations for determining the bias point in an *npn* CC configuration are

$$\begin{aligned} &V_{BE} = 0.7\text{ V (Si)},\quad 0.3\text{ V (Ge)} \\ &I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E} \\ &I_E = (\beta + 1) I_B \approx \frac{V_{CC} - V_{BE}}{R_E + \dfrac{R_B}{\beta}} \approx I_C \\ &V_{CE} = V_{CC} - I_E R_E \end{aligned} \qquad (4\text{–}28)$$

In most situations, we are normally concerned only with the collector (or emitter) current and the collector–emitter voltage. So the approximation in equations 4–28 for I_C or I_E can give a quick answer without need for calculating I_B. For a *pnp* CC bias circuit, use the absolute value of V_{CC}, V_{BE}, and V_{CE}.

EXAMPLE 4–12

a. Find the bias point of the germanium transistor in the circuit of Figure 4–43. Assume that $\beta = 120$.

Solution

From equations 4–28,

$$V_{BE} = 0.3\text{ V}$$

$$I_B = \frac{16\text{ V} - 0.3\text{ V}}{116.5 \times 10^3\ \Omega + 121 \times 10^3\ \Omega} = 66.105\ \mu\text{A}$$

$$I_E = (121)(66.105\ \mu\text{A}) = 8\text{ mA}\ (7.97\text{ mA using the approximation})$$

$$V_{CE} = 16\text{ V} - (8 \times 10^{-3}\text{ A})(10^3\ \Omega) = 8\text{ V}$$

b. Determine the bias point for the *pnp* circuit shown in Figure 4–43(b). Compare your answers to part (a).

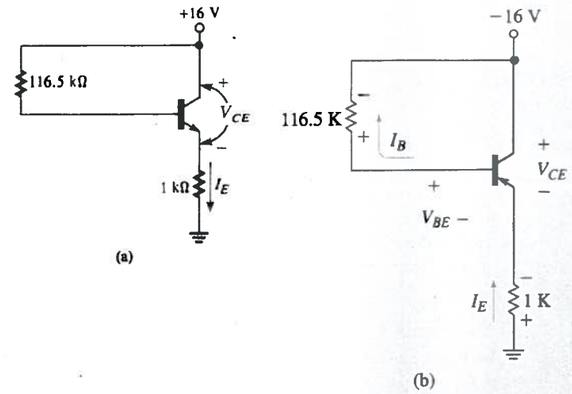
Solution

Write the KVL equations for the circuit shown in Figure 4–43(b).

$$-V_{CC} + I_B R_B - V_{BE} - I_E R_E = 0$$

$$-V_{CC} + I_B R_B - V_{BE} - (\beta + 1) I_B R_E = 0$$

FIGURE 4–43 (Example 4–12)



$$-V_{CC} + I_B[R_B + (\beta + 1)R_E] - V_{BE} = 0$$

$$I_B = \frac{V_{CC} + V_{BE}}{R_B + (\beta + 1)R_E} = \frac{16 - 0.3}{116.5\text{ k} + (121)(1\text{ k})} = 66.11\ \mu\text{A}$$

To solve for V_{CE}:

$$I_E = (\beta + 1)I_B = (120 + 1)66.105\ \mu\text{A} = 8\text{ mA}$$

and

$$V_{CE} = -16 + (8\text{ mA})(1\text{ k}) = -8.0\text{ V}$$

V_{CE} is negative as expected.

Note that the values obtained for the *npn* and *pnp* transistors are the same. These values should be the same because the same component values are used and the betas for each transistor are the same. The process just described illustrates the use of KVL with the appropriate signs to solve for I_E and V_{CE}. In practice, we can simply write

$$I_C \approx I_E \approx \frac{|V_{CC}| - |V_{BE}|}{R_E + \frac{R_B}{\beta}}$$

$$\text{and } |V_{CE}| = |V_{CC}| - I_E R_E$$

4–7 DESIGN CONSIDERATIONS

CB Bias Design

Design is nothing more than "backwards" analysis. In other words, using equations and formulas derived through analysis in order to find items such as resistor values and power supply voltages. Although a bias circuit for the common-base configuration can be designed using a single dc power supply, we will consider only the two-source design (Figure 4–28) at this point in our discussion. In the usual design scenario, the supply voltages V_{EE} and V_{CC} are fixed, and we must choose values for R_E and R_C to obtain a specified bias current I_E and bias voltage V_{CB}. Letting $I_C = I_E$, equations 4–21 are easily solved for R_E and R_C in terms of I_E and V_{CB}:

$$R_E = \frac{V_{EE} - V_{EB}}{I_E} \qquad R_C = \frac{V_{CC} - V_{CB}}{I_E} \tag{4–29}$$

In practical discrete-circuit designs, it is often necessary to use standard-valued resistors. The standard values closest to the values calculated from equations 4–29 are used, and the circuit is analyzed to determine the resulting values of I_E and V_{CB}. If variation from the desired bias values is a critical consideration in a particular application, it may be necessary to use precision resistors or to calculate the total possible variation that could arise from using resistors that have a specified tolerance. The next example demonstrates these ideas.

EXAMPLE 4–13

A common-base bias circuit is to be designed for an *npn* silicon transistor to be used in a system having dc power supplies +15 V and −5 V. The bias point is to be $I_E = 1.5$ mA and $V_{CB} = 7.5$ V.

DESIGN

1. Design the circuit, using standard-valued resistors with 5% tolerance.
2. What are the actual bias values if the resistors selected have their nominal values?
3. What are the possible ranges of I_E and V_{CB}, taking the resistor tolerances into consideration?

Solution

1. From equations 4–29,

$$R_E = \frac{(5 - 0.7)\text{ V}}{1.5 \times 10^{-3}\text{ A}} = 2867\ \Omega$$

$$R_C = \frac{(15 - 7.5)\text{ V}}{1.5 \times 10^{-3}\text{ A}} = 5000\ \Omega$$

Appendix B contains a table of the standard values of resistors having 5% and 10% tolerances. The standard 5% resistors with values closest to those calculated for R_E and R_C are $E_E = 3\text{ k}\Omega$ and $R_C = 5.1\text{ k}\Omega$.

2. From equations 4–21,

$$I_E = \frac{(5 - 0.7)\text{ V}}{3\text{ k}\Omega} = 1.43\text{ mA}$$

$$V_{CB} = 15\text{ V} - (1.43\text{ mA})(5.1\text{ k}\Omega) = 7.69\text{ V}$$

3. The ranges of possible resistance values for R_E and R_C are

$$R_E = 3\text{ k}\Omega \pm 0.05(3\text{ k}\Omega) = 2850\text{–}3150\ \Omega$$

$$R_C = 5.1\text{ k}\Omega \pm 0.05(5.1\text{ k}\Omega) = 4845\text{–}5355\ \Omega$$

$$I_{E(min)} = \frac{V_{EE} - V_{BE}}{R_{E(max)}} = \frac{(5 - 0.7)\text{ V}}{3150\ \Omega} = 1.365\text{ mA}$$

$$I_{E(max)} = \frac{V_{EE} - V_{BE}}{R_{E(min)}} = \frac{(5 - 0.7)\text{ V}}{2850\ \Omega} = 1.509\text{ mA}$$

$$V_{CB(min)} = V_{CC} - I_{E(max)}R_{C(max)} = 15\text{ V} - (1.509\text{ mA})(5355\ \Omega) = 6.92\text{ V}$$

$$V_{CB(max)} = V_{CC} - I_{E(min)}R_{C(min)} = 15\text{ V} - (1.365\text{ mA})(4845\ \Omega) = 8.39\text{ V}$$

We see that considerable variation from the desired bias point is possible when using standard-valued resistors.

CE Bias Design

In Chapter 7 we discuss the design of a voltage-divider bias circuit that has certain properties superior to the design shown in Figure 4–33. However, when simplicity and minimization of the number of components are the primary considerations, the circuit of Figure 4–33 is used. Assuming the supply voltage V_{CC} is fixed, we solve equations 4–24 for R_B and R_C in terms of the desired bias values for I_C and V_{CE}:

$$R_B = \frac{V_{CC} - V_{BE}}{I_C/\beta} \qquad R_C = \frac{V_{CC} - V_{CE}}{I_C} \tag{4–30}$$

The practical difficulty with this design is that the bias point depends heavily on the value of β, which varies considerably with temperature. Also, there is typically a wide variation in the value of β among transistors of the same type. Consequently, this design is not recommended for applications where wide temperature variations may occur or for volume production (where different transistors are used). The next example demonstrates this point.

EXAMPLE 4–14

DESIGN

An *npn* silicon transistor having a nominal β of 100 is to be used in a CE configuration with $V_{CC} = 12$ V. The bias point is to be $I_C = 2$ mA and $V_{CE} = 6$ V.

1. Design the circuit, using standard-valued 5% resistors.
2. Find the range of possible bias values if the β of the transistor can change to any value between 50 and 150 (a typical range). Assume that the 5% resistors have their nominal values.

Solution

1. From equations 4–30,

$$R_B = \frac{(12 - 0.7)\text{ V}}{2 \times 10^{-3}\text{A}/100} = 565\text{ k}\Omega$$
$$R_C = \frac{(12 - 6)\text{ V}}{2 \times 10^{-3}\text{ A}} = 3\text{ k}\Omega$$

From Appendix B, the standard 5% resistors having values closest to those calculated are $R_B = 560$ kΩ and $R_C = 3$ kΩ.

2. From equations 4–24,

$$I_B = \frac{(12 - 0.7)\text{ V}}{560\text{ k}\Omega} = 20.18\ \mu\text{A}$$
$$I_{C(min)} = \beta_{(min)} I_B = 50(20.18\ \mu\text{A}) = 1.01\text{ mA}$$
$$I_{C(max)} = \beta_{(max)} I_B = 150(20.18\ \mu\text{A}) = 3.03\text{ mA}$$
$$V_{CE(min)} = V_{CC} - I_{C(max)} R_C = 12\text{ V} - (3.03\text{ mA})(3\text{ k}\Omega) = 2.92\text{ V}$$
$$V_{CE(max)} = V_{CC} - I_{C(min)} R_C = 12\text{ V} - (1.01\text{ mA})(3\text{ k}\Omega) = 8.97\text{ V}$$

In most practical applications, the possible variation of V_{CE} from 2.92 V to 8.97 V would be intolerable.

CC Bias Design

To obtain resistor values for the common-collector bias circuit (Figure 4–41), we solve equations 4-28 for R_E and R_B in terms of the desired bias values I_E and V_{CE}:

$$R_E = \frac{V_{CC} - V_{CE}}{I_E}$$
$$R_B = \frac{(\beta + 1)}{I_E}(V_{CC} - V_{BE} - I_E R_E) \approx \beta\left(\frac{V_{CC} - V_{BE}}{I_E} - R_E\right) \qquad (4\text{–}31)$$

EXAMPLE 4–15

DESIGN

An *npn* silicon transistor having β = 100 is to be used in a CC configuration with $V_{CC} = 24$ V. The desired bias point is $V_{CE} = 16$ V and $I_E = 4$ mA.

1. Design the bias circuit using standard-valued 5% resistors.
2. Find the actual bias point when the standard resistors are used, assuming they have their nominal values.

Solution

1. From equation 4–31,

$$R_E = \frac{(24 - 16)\text{V}}{4\text{ mA}} = 2\text{ k}\Omega$$
$$R_B = \frac{101}{4 \times 10^{-3}\text{ A}}[24\text{ V} - 0.7\text{ V} - (4\text{ mA})(2\text{ k}\Omega)] = 386.3\text{ k}\Omega$$

or

$$R_B \approx 100\left(\frac{24 - 0.7}{4 \times 10^{-3}} - 2\text{k}\right) = 382.5\text{ k}\Omega$$

From Appendix B, the standard 5% resistors having values closest to those calculated are $R_E = 2$ kΩ and $R_B = 390$ kΩ.

2. From equations 4–28,

$$I_B = \frac{(24 - 0.7)\text{ V}}{390\text{ k}\Omega + 101(2\text{ k}\Omega)} = 39.358\ \mu\text{A}$$
$$I_E = 101(39.358\ \mu\text{A}) = 3.98\text{ mA}$$
$$V_{CE} = 24\text{ V} - (3.98\text{ mA})(2\text{ k}\Omega) = 16.04\text{ V}$$

4–8 THE BJT INVERTER (TRANSISTOR SWITCH)

Transistors are widely used in digital logic circuits and switching applications. Recall that the waveforms encountered in those applications periodically alternate between a "low" and a "high" voltage, such as 0 V and +5 V. The fundamental transistor circuit used in switching applications is called an *inverter*, the *npn* version of which is shown in Figure 4–44. Note in the figure that the transistor is in a common-emitter configuration, but there is no bias voltage connected to the base through a resistor, as in the CE bias circuits studied earlier. Instead, a resistor R_B is connected in series with the base and then directly to a square or pulse-type waveform that serves as the inverter's input. In the circuit shown, V_{CC} and the "high" level of the input are both +5 V. The output is the voltage between collector and emitter (V_{CE}), as usual.

When the input to the inverter is high (+5 V), the base–emitter junction is forward biased and current flows through R_B into the base. The values of

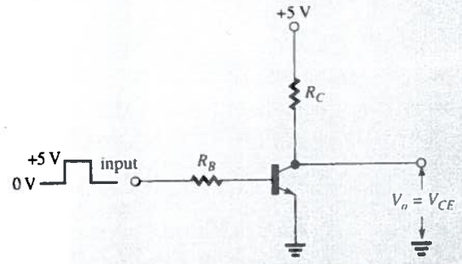


FIGURE 4–44 An *npn* transistor inverter, or switch

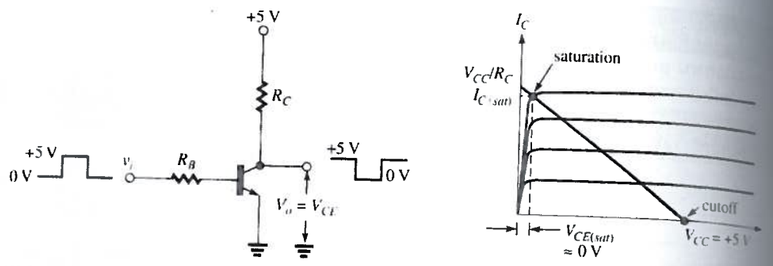


FIGURE 4–45 When the input to the inverter is high (+5 V), the transistor is saturated and its output is low (≈ 0 V). When the input to the inverter is low, the transistor is cut off and its output is high.

R_B and R_C are chosen (designed) so that the amount of base current flowing is enough to *saturate* the transistor, that is, to drive it into the saturation region of its output characteristics. Figure 4–45 shows a load line plotted on a set of CE output characteristics and identifies the point on the load line where saturation occurs. Note that the value of V_{CE} corresponding to this point, called $V_{CE(sat)}$, is very nearly 0 (typically about 0.1 V). The current at the saturation point is called $I_{C(sat)}$ and is very nearly equal to the intercept of the load line of the I_C-axis, namely, V_{CC}/R_C. When the transistor is saturated, it is said to be *ON*. This analysis has shown that a high input to the inverter (+5 V) results in a low output (≈ 0 V).

When the input to the transistor is low, that is, 0 V, the base–emitter junction has no forward bias applied to it, so no base current, and hence no collector current, flows. There is, therefore, no voltage drop across R_C, and it follows that V_{CE} must be the same as V_{CC}: +5 V. This fact is made evident by substituting $I_C = 0$ in the equation for V_{CE} (equation 4–24): $V_{CE} = V_{CC} - I_C R_C = V_{CC} - (0)(R_C) = V_{CC}$. In this situation, the transistor is in the cutoff region of its output characteristics, as shown in Figure 4–45, and is said to be *OFF*. A low input to the inverter results in a high output, and it is now obvious why this circuit is called an *inverter*.

In designing and analyzing transistor inverters, it is usually assumed that $I_{C(sat)} = V_{CC}/R_C$ and that $V_{CE(sat)} = 0$ V. These are very good approximations and lead to results that are valid for most practical applications. Under these assumptions, we can easily derive the voltage–current relations in a transistor inverter. Because the transistor is cut off when the input is low, regardless of the values of R_B and R_C, the equations we will study are those that apply when the input is high. Actually, these equations are precisely those we have already derived for a CE transistor, for the special case $I_C = I_{C(sat)}$. Thus, assuming saturation exists,

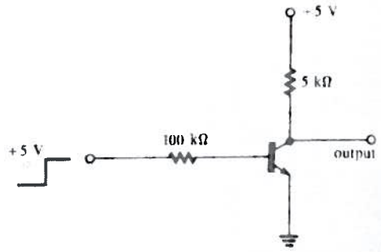
$$I_C = I_{C(sat)} = \frac{V_{CC}}{R_C} \tag{4–32}$$

$$I_B = \frac{I_{C(sat)}}{\beta} = \frac{V_{CC}}{\beta R_C} \tag{4–33}$$

$$I_B = \frac{V_{HI} - V_{BE}}{R_B} \tag{4–34}$$

where V_{HI} is the high level of the input voltage, usually the same as V_{CC}.

FIGURE 4–46 (Example 4–16)



Regarding Equation 4–33, some books use the notation $I_{B(sat)} = \dfrac{I_{C(sat)}}{\beta}$ where $I_{B(sat)}$ is the minimum I_B necessary for saturation.

EXAMPLE 4–16

Verify that the circuit in Figure 4–46 behaves like an inverter when the input switches between 0 V and +5 V. Assume that the transistor is silicon and that $\beta = 100$.

Solution

It is only necessary to verify that the transistor is saturated when $V_i = +5$ V. From equation 4–34.

$$I_B = \frac{(5 - 0.7)\text{ V}}{100\text{ k}\Omega} = 43\ \mu\text{A}$$

Then

$$I_C = \beta I_B = 100(43\ \mu\text{A}) = 4.3\text{ mA}$$

and

$$V_{CE} = 5 - (4.3\text{ mA})(5\text{ k}\Omega) = 5 - 21.5 = -16.5\text{ V}$$

A negative V_{CE} indicates that the transistor is indeed in saturation and that $V_{CE} = V_{CE(sat)} \approx 0$ V, and $I_C = I_{C(sat)} \approx \dfrac{V_{CC}}{R_C} = 1$ mA. We could have concluded that the transistor was in saturation by calculating $I_{C(sat)} \approx V_{CC}/R_C$ and comparing it to the calculated I_C of 4.3 mA. When $I_C = \beta I_B$ is greater than $I_{C(sat)}$, saturation occurs. We can also determine saturation by comparing base currents. The minimum base current necessary to saturate is $I_B = \dfrac{V_{CC}}{\beta R_B}$. In this example, $\dfrac{V_{CC}}{\beta R_C} = \dfrac{5}{100(5\text{k})} = 10\ \mu$A. Since $I_B = 43\ \mu\text{A} > 10\ \mu\text{A}$, the transistor is in saturation. If we changed R_B to, say, 750 kΩ, the resulting base current would be 5.73 μA and the transistor would not be saturated. The collector current would then be 0.573 mA and V_{CE} would be 2.13 V.

Inverter Design

To design a transistor inverter we must have criteria for specifying the values of R_B and R_C. Typically, one of the two is known (or chosen arbitrarily), and the value of the other is derived from the first. Using equations 4–33 and 4–34, we can obtain the following relationships between R_B and R_C:

$$R_B = \frac{V_{HI} - V_{BE}}{I_B} = \frac{(V_{HI} - V_{BE})\beta R_C}{V_{CC}} \tag{4–35}$$

$$R_C = \frac{V_{CC}R_B}{\beta(V_{HI} - V_{BE})} \tag{4–36}$$

Equation 4–35 can be used to find R_B when R_C is known, and equation 4–36 to find R_C when R_B is known. However, because these equations are valid only for a specific value of β, they are not entirely practical. We have already discussed the fact that the β of a transistor of a given type is likely to vary over a wide range. If the actual value of β is smaller than the one used in the design equations, the transistor will not saturate. For this reason, the β used in the design equations should always be the *smallest* possible value that might occur in a given application. In other words, equations 4–35 and 4–36 are more practical when expressed in the form of inequalities, as follows:

$$R_B \leq \frac{(V_{HI} - V_{BE})\beta R_C}{V_{CC}} \tag{4–37}$$

$$R_C \geq \frac{V_{CC}R_B}{\beta(V_{HI} - V_{BE})} \tag{4–38}$$

These inequalities should hold for the entire range of β-values that transistors used in the inverter may have. This will be the case if the minimum possible β-value is used.

We should note that when a transistor has a higher value of β than the one for which the inverter circuit is designed, a high input simply drives it deeper into saturation. This *overdriving* of the transistor creates certain new problems, including the fact that it slows the speed at which the device can switch from ON to OFF, but the output is definitely low in the ON state. The results from Example 4–16 indicate an overdriving condition, because I_B was about four times larger than the minimum required. In practice, however, a moderate amount of overdriving is normally used in order to maintain a low $V_{CE(sat)}$.

EXAMPLE 4–17

DESIGN

An inverter having $R_C = 1.5\ \text{k}\Omega$ is to be designed so that it will operate satisfactorily with silicon transistors whose β-values range from 80 to 200. What value of R_B should be used? Assume that $V_{CC} = V_{HI} = +5\,\text{V}$.

Solution

Using equation 4–35 with $\beta = \beta_{(\text{min})} = 80$, we find

$$R_B \leq \frac{(V_{HI} - V_{BE})\beta_{(\text{min})}R_C}{V_{CC}} = \frac{(4.3)(80)(1.5\ \text{k}\Omega)}{5} = 103.2\ \text{k}\Omega$$

An actual value of 100 kΩ would be appropriate.

The Transistor as a Switch

A transistor inverter is often called a transistor *switch*. This terminology is appropriate because the ON and OFF states of the transistor correspond closely to the closing and opening of a switch connected between the collector and the emitter. When the transistor is ON, or saturated, the voltage between collector and emitter is nearly 0, as it would be across a closed switch, and the current is the maximum possible, V_{CC}/R_C. When the transistor is OFF, no current flows from collector to emitter and the voltage is maximum, as it would be across an open switch. The switch is opened or closed by the input voltage: A high input closes it and a low input opens it. Figure 4–47 illustrates these ideas.

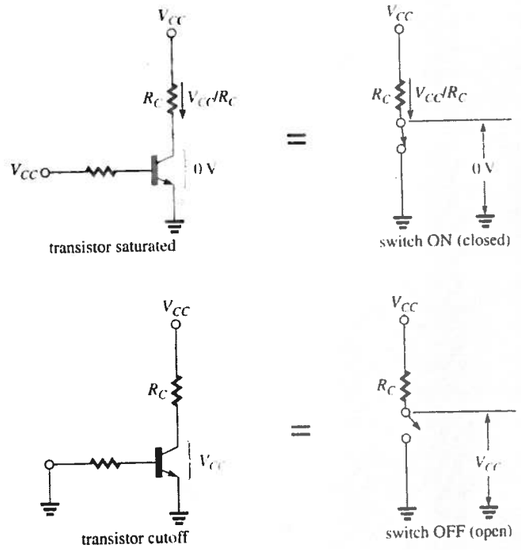


FIGURE 4–47 The transistor as a voltage-controlled switch. A high input closes the switch and a low input opens it.

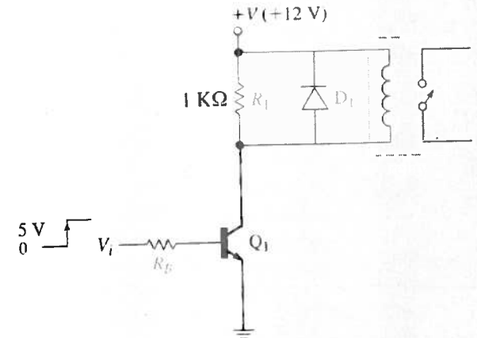


FIGURE 4–48 The BJT inverter interfaced to a relay. V_i is a TTL-level logic voltage.

In many switching applications, the emitter may be connected to another circuit, or to another voltage source, instead of to ground. When analyzing such complex digital circuits, it is quite helpful to think of the transistor as simply a switch, for then it is easy to understand circuit operation in terms of the collector circuit being connected to or disconnected from the emitter circuit. For example, if the emitter in the basic inverter circuit were connected to −5 V instead of ground, then the output would clearly switch between +5 V and −5 V instead of between +5 V and 0 V.

A popular use of the BJT inverter is for interfacing logic signals to electromechanical devices such as relays. BJT transistors interface well to relays because they can easily sink the required current to fully turn on a relay's magnetic coil. A schematic of a BJT interfaced to a relay is shown in Figure 4–48.

The input to this circuit is a digital logic signal. The logical high-level voltage in digital signals varies considerably. Do not assume that a logical high is 5.0 V. Many of the new digital systems are using 3.3 V for a logical high. Also, for TTL 5.0-V logic systems, a logical high voltage can vary from 2.5 V to 5.0 V. When in doubt, measure the voltage level of your system. Second, the

relay should turn on when the logic level is "high," and, accordingly, the relay will turn off when the input logic level is "low." The following is a summary of considerations for designing the relay interface:

1. TTL logic levels are not exact.
2. Transistor switching speed is not usually an issue when turning a relay on/off.
3. The β of the transistor is not usually known unless you take time to measure it.

Design Procedure

1. Determine the logic-level voltage you want for the transistor and relay to turn on. This should be some value that the logic level is guaranteed to reach. For a 5.0-V TTL system, 3.0 V is usually a guaranteed value. If you select a value such as 4.5 V, the transistor might not fully saturate, which could cause the relay coil to not fully energize. This could cause erratic behavior of the relay.
2. Recall that in many cases, the β of the transistor is not known. Of course, the user could set up a test or use a curve tracer to extract the β value for calculating R_B. For typical TTL logic levels, a resistor of about 1 kΩ to 5 kΩ for R_B works very well.
3. When the input logic level is low, the transistor will be placed in the cut-off condition ($I_C \cong 0$). This is called the *open collector* condition. To fully turn off the relay, a pull-up resistor (R_C) is connected across the relay.
4. When the transistor is ON, a current will be flowing in the magnetic coil. Recall that inductances store energy in terms of current. When the transistor is turned OFF, the coil will attempt to de-energize through the pull-up resistor R_C, which can lead to a significantly large voltage spike (transient). This transient can cause glitches in logic levels and can damage the circuits. This problem can be minimized by placing a reversed-biased diode (D_1) across the coil of the relay, as shown in Figure 4–48. D_1 will clamp any voltage on the collector to a maximum value of 0.7 V by providing a low-resistance path for the coil to de-energize. The diodes are also quick reacting, and the junction capacitance in the diode helps to suppress the back EMF induced by the de-energizing coil.

Q_1 is used to turn the relay on/off. Recall that when Q_1 is saturated, $V_{CE} \approx 0.1$ V (very close to 0). Typical transistors for relays requiring 50 mA or less are the 2N3904 and 2N2222, although many other transistors are suitable. The circuit is shown in Figure 4–48.

4–9 TRANSISTOR TYPES, RATINGS, AND SPECIFICATIONS

In modern electronic circuits, discrete transistors are used primarily for applications in which only one or a small number of devices are required and in applications where substantial power is dissipated. Although older designs, composed entirely of discrete devices, can still be found in large numbers, most new circuits containing a large number of transistors are constructed in integrated-circuit form. In many applications, both discrete and integrated components are used. In these applications, the integrated circuit typically performs complex, low-level *signal conditioning*, and a discrete transistor then drives a power-consuming load such as an indicator lamp or an audio speaker. This use of the transistor is an example of *interfacing;* it

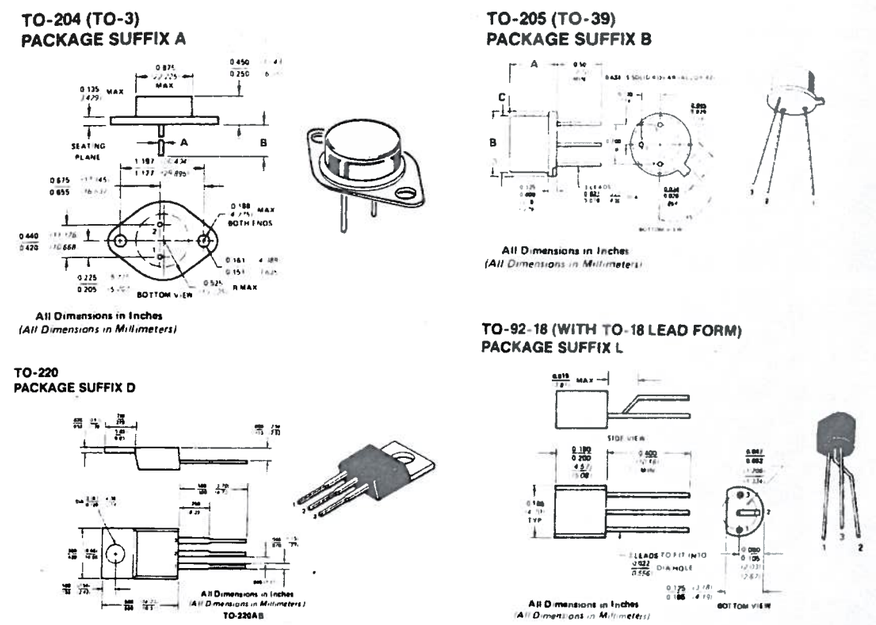


FIGURE 4–49 A few of the standard transistor case (enclosure) types, with TO-designations (old JEDEC) numbers in parentheses (Courtesy of Siliconix Inc.)

provides a link between a device having limited power capabilities and a load that requires large voltages or currents.

Discrete transistors are packaged in a wide variety of metal and plastic enclosures (cases). Figure 4–49 shows some of the standard case types, which are identified by standard TO numbers. Three leads are brought out through each enclosure to permit external connection to the transistor's emitter, base, and collector. In some power transistors, rated for high power dissipation, the collector is attached and electrically common to the metal case. (The majority of the power dissipated in a transistor occurs at the collector–base junction, since the collector voltage is usually the largest voltage in the device.) A transistor manufacturer uses a consistent scheme that can be followed to identify the base, emitter, and collector terminals for a given case type. For example, in the TO-39 case, the three leads are attached in a semicircular cluster and a metal tab on the case is adjacent to the emitter. The base is the center lead in the cluster, and the collector is the remaining lead.

A discrete transistor of a specific type, having registered JAN (military) specifications, is identified by a number with the prefix 2N. Although all transistors having the same number may not be identical, they are all designed to meet the same performance specifications related to voltage and current limits, power dissipation, operating temperature range, and parameter variations. More than one manufacturer may produce a transistor with a given 2N number. Many manufacturers also produce "commercial"-grade devices that do not have 2N designations.

Figure 4–50 shows parts of a typical set of manufacturer's transistor specifications. The maximum ratings show the maximum voltages that each device can sustain between different sets of transistor terminals and the maximum power dissipation, P_D, at 25°C. The effect of temperature on

FIGURE 4–50 Typical transistor specifications for electrical (dc) characteristics and beta (h_{FE}) variation (Courtesy of ON Semiconductor)

MPS2222, MPS2222A

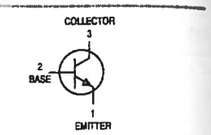
MPS2222A is a Preferred Device

General Purpose Transistors

NPN Silicon

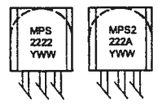
ON Semiconductor

http://onsemi.com



TO–92
CASE 29
STYLE 1

MARKING DIAGRAMS



Y = Year
WW = Work Week

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage MPS2222 / MPS2222A	V_{CEO}	30 / 40	Vdc
Collector–Base Voltage MPS2222 / MPS2222A	V_{CBO}	60 / 75	Vdc
Emitter–Base Voltage MPS2222 / MPS2222A	V_{EBO}	5.0 / 6.0	Vdc
Collector Current – Continuous	I_C	600	mAdc
Total Device Dissipation @ T_A = 25°C; Derate above 25°C	P_D	625; 5.0	mW; mW/°C
Total Device Dissipation @ T_C = 25°C; Derate above 25°C	P_D	1.5; 12	Watts; mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150	°C

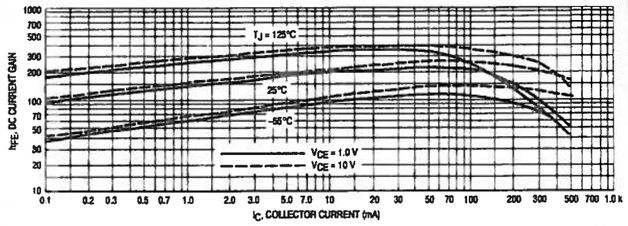


Figure 3. DC Current Gain

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)	MPS2222 / MPS2222A	$V_{(BR)CEO}$	30 / 40	–	Vdc
Collector–Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	MPS2222 / MPS2222A	$V_{(BR)CBO}$	60 / 75	–	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	MPS2222 / MPS2222A	$V_{(BR)EBO}$	5.0 / 6.0	–	Vdc
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 3.0 Vdc)	MPS2222A	I_{CEX}	–	10	nAdc
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 50 Vdc, I_E = 0)	MPS2222		–	0.01	
(V_{CB} = 60 Vdc, I_E = 0)	MPS2222A		–	0.01	
(V_{CB} = 50 Vdc, I_E = 0, T_A = 125°C)	MPS2222		–	10	
(V_{CB} = 50 Vdc, I_E = 0, T_A = 125°C)	MPS2222A		–	10	
Emitter Cutoff Current (V_{EB} = 3.0 Vdc, I_C = 0)	MPS2222A	I_{EBO}	–	100	nAdc
Base Cutoff Current (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 3.0 Vdc)	MPS2222A	I_{BL}	–	20	nAdc
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			–
(I_C = 0.1 mAdc, V_{CE} = 10 Vdc)			35	–	
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc)			50	–	
(I_C = 10 mAdc, V_{CE} = 10 Vdc)			75	–	
(I_C = 10 mAdc, V_{CE} = 10 Vdc, T_A = –55°C)	MPS2222A only		35	–	
(I_C = 150 mAdc, V_{CE} = 10 Vdc) (Note 1.)			100	300	
(I_C = 150 mAdc, V_{CE} = 1.0 Vdc) (Note 1.)			50	–	
(I_C = 500 mAdc, V_{CE} = 10 Vdc) (Note 1.)	MPS2222		30	–	
	MPS2222A		40	–	
Collector–Emitter Saturation Voltage (Note 1.)		$V_{CE(sat)}$			Vdc
(I_C = 150 mAdc, I_B = 15 mAdc)	MPS2222		–	0.4	
	MPS2222A		–	0.3	
(I_C = 500 mAdc, I_B = 50 mAdc)	MPS2222		–	1.6	
	MPS2222A		–	1.0	
Base–Emitter Saturation Voltage (Note 1.)		$V_{BE(sat)}$			Vdc
(I_C = 150 mAdc, I_B = 15 mAdc)	MPS2222		–	1.3	
	MPS2222A		0.6	1.2	
(I_C = 500 mAdc, I_B = 50 mAdc)	MPS2222		–	2.6	
	MPS2222A		–	2.0	

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

transistor specifications will be covered in detail in Chapter 16 (Section 16–3). A transistor circuit designer must be certain that a transistor used in a particular application will not be subjected to voltages or power dissipations that exceed the specified maximums; failure to do so may result in severe performance degradation or permanent damage.

The graph labeled "DC Current Gain" shows how β varies with V_{CE}, junction temperature (T_J), and collector current. (In the CE configuration, current *gain* is the ratio of output current to input current, or I_C/I_B, which is approximately β. As we shall learn later when h parameters are discussed, β is also designated by h_{FE}.) The chart illustrates a typical transistor characteristic: For a fixed collector current, *the value of* β *increases with increasing temperature.*

The *electrical characteristics* listed in Figure 4–50 show important transistor parameters associated with the dc operation of each device. Included are breakdown voltages and reverse leakage currents (called "cutoff" currents in the specifications). Notice that the breakdown voltages previously referred to as BV_{CBO} and BV_{CEO} are listed as $V_{BR(CBO)}$ and $V_{BR(CEO)}$, respectively.

Figure 4–50 does not show some other specifications that are usually furnished by a manufacturer, including small-signal characteristics. Small-signal characteristics are associated with the ac operation of a transistor, which we will cover in Chapter 7. Other specifications often furnished by the manufacturer include graphs showing additional parameter variations with temperature, voltage, and current.

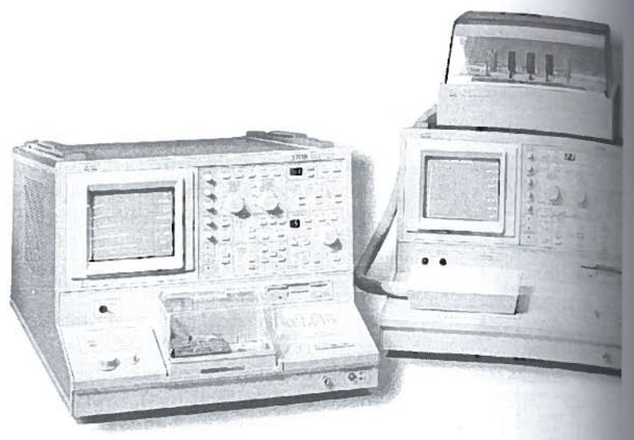
4–10 TRANSISTOR CURVE TRACERS

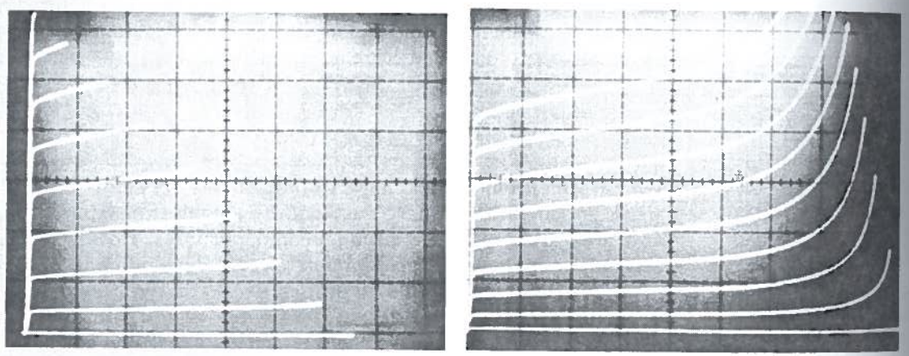
We have mentioned that characteristic curves are seldom included in transistor specifications. These vary widely among transistors of a given type and are rarely used for circuit design purposes. However, in areas such as component testing, preliminary circuit development, and research, it is often useful to be able to study the characteristic curves of a single device and to obtain important parameter values from the curves. Recall that parameters such as α, β, BV_{CBO}, BV_{CEO}, leakage currents, saturation voltages, and the Early voltage can be discerned from appropriate sets of characteristic curves.

The most widely used method for obtaining a set of characteristic curves is by use of an instrument called a *transistor curve tracer.* A curve tracer is basically an oscilloscope equipped with circuitry that automatically steps the currents (or voltages) in a semiconductor device through a range of values and displays the family of characteristic curves that result. Selector switches allow the user to set the maximum value and the increment (step) value of each current or voltage applied to the device. For example, to obtain a family of transistor collector characteristics, the user might set the base current increment to be 10 μA, the maximum collector voltage to be 25 V, and the number of steps to be 10. The characteristics would then be displayed as a family of curves showing I_C versus V_{CE} for I_B = 0, 10 μA, 20 μA, ... Figure 4–51 shows two typical curve tracers.

Figure 4–52(a) is a photograph of a curve tracer display showing a typical set of *npn* collector characteristics. The horizontal sensitivity of the display was set for 2 V/division, so the horizontal axis (V_{CE}) extends from 0 to about 13 V. The vertical sensitivity was set for 1 mA/division, so the vertical axis (I_C) extends from 0 to about 6.5 mA. The base current increment is 10 μA. Using this display, we can determine, for example, that the β of the transistor at V_{CE} = 4 V and I_B = 40 μA is approximately

FIGURE 4–51 Two typical curve tracers (Tektronix Models 370B and 371B) (Courtesy of Tektronix, Inc.)





(a) Horizontal: 2 V/div
Vertical: 1 mA/div
ΔI_B = 10 μA

(b) Horizontal: 2 V/div
Vertical: 0.2 mA/div
ΔI_B = 2 μA

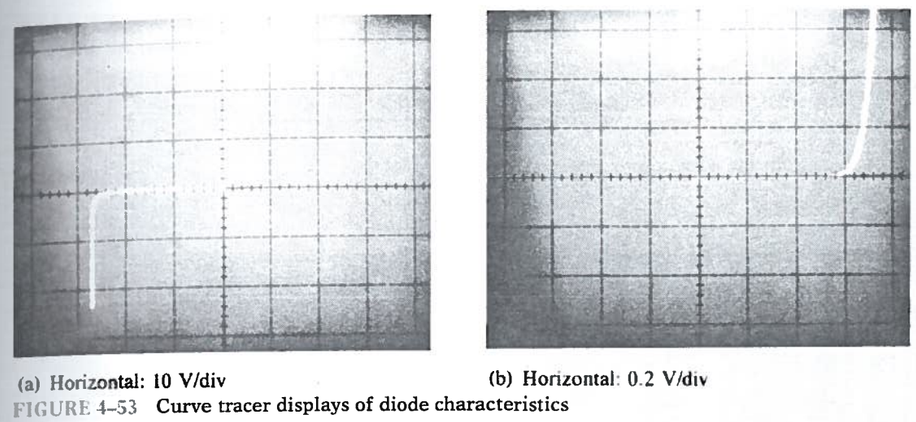
FIGURE 4–52 Photographs of curve tracer displays

$$\beta = \frac{I_C}{I_B} = \frac{3\text{ mA}}{40\ \mu\text{A}} = 75$$

The curve tracer from which this display was obtained permits the user to select a value of series collector resistance (R_C), which, for the display shown, was set to 2 kΩ. Notice that the base current curves become shorter with increasing current. *An imaginary line connecting the right-hand tips of each curve represents the load line for the circuit.* This load line is seen to intersect the V_{CE}-axis at 13 V and the I_C-axis at 6.5 mA. Thus, the value of V_{CC} used in this circuit is 13 V, and the load line intersects the I_C-axis at the value expected:

$$I_C = \frac{V_{CC}}{R_C} = \frac{13\text{ V}}{2\text{ k}\Omega} = 6.5\text{ mA}$$

One convenient feature of a curve tracer is that it permits a user to expand or contract the display in different regions of the characteristic curves by adjusting the sensitivity and range controls.



(a) Horizontal: 10 V/div

(b) Horizontal: 0.2 V/div

FIGURE 4–53 Curve tracer displays of diode characteristics

Figure 4–52(b) shows collector characteristics of the same transistor when the curve tracer settings are adjusted to generate larger values of V_{CE}. In this example, the horizontal sensitivity is 2 V/division, the vertical sensitivity is 0.2 mA/division, and the base current increment is 2 μA. With these settings, the breakdown characteristics are clearly evident. For example, at I_B = 12 μA and V_{CE} = 12 V, it can be seen that the transistor is in its breakdown region and that the collector current is approximately 0.84 mA.

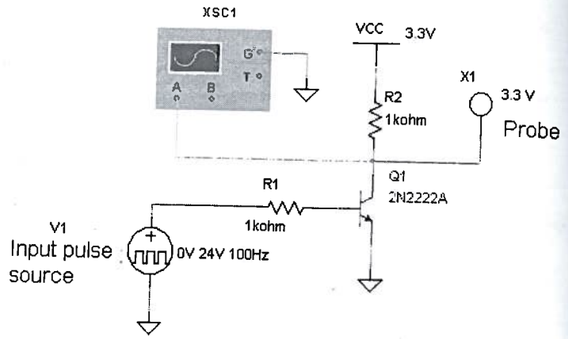
Most curve tracers can be used to obtain characteristic curves for devices other than transistors. Some even have special adapters that allow the testing of integrated circuits. Figure 4–53 shows photographs of diode characteristics that were obtained from a curve tracer display. The forward and reverse characteristics are shown in Figure 4–53(a), with a horizontal sensitivity of 10 V/division. It can be seen that the diode enters breakdown at a reverse voltage of about 25 V. With this scale, the forward characteristic essentially coincides with the vertical axis. However, when the sensitivity is set to 0.2 V/division, the forward characteristic appears as shown in Figure 4–53(b) and can be examined in detail. (The origin of the axes is at the center of the display.) We see that the knee of the characteristic occurs at about 0.62 V, and there is sufficient detail to compute dc and ac resistances in the forward region.

4–11 BJT CIRCUIT ANALYSIS WITH ELECTRONICS WORKBENCH MULTISIM

This section examines the use of EWB to simulate a transistor switch circuit. The transistor switch circuit is probably one of the most useful functions of a discrete BJT transistor. The transistor has plenty of drive current capability for driving most relays or even providing level conversion. For example, a signal that switches between +24 and ground can easily be converted to a +3.3/0.0 switching voltage level using a discrete BJT transistor. This section demonstrates how to simulate this circuit with EWB.

This chapter introduced the basic concepts of transistor operation. The student learned that the BJT transistor has three modes of operation: cutoff, active, and saturation. The BJT switch operates primarily in either the cutoff or saturation regions. In the cutoff region, $I_C \approx 0$ and $V_{CE} = V_{CC}$. In the saturation mode, $I_C = V_{CC}/R_C$ and V_{CE} = 0.0 V. You also learned that resistor values of 1 kΩ work well for R_B and R_C in most applications. The objective of this section are as follows:

FIGURE 4–54 The EWB Multisim circuit



- Use EWB to construct a BJT switch circuit and verify that the circuit switches between the specified voltages.
- Develop an understanding on how to set the probe threshold voltage value and set the pulse parameters on a pulse voltage source.

Open the circuit **Ch4_EWB.msm** found in the Electronics Workbench CD-ROM packaged with the text. This file is the simple switch circuit (shown in Figure 4–54) containing a +24-V input switching signal, a 2N2222 BJT-NPN transistor, +3.3-V voltage source, two 1-kΩ resistors, and a Multisim probe (X1) that has been triggered to turn on at 3.3 volts.

The settings for the probe are obtained by double-clicking on the probe icon, selecting the value tab, and then setting the threshold voltage to 3.3 V (Figure 4–55). The menu for setting the probe values is provided in Figure 4–56.

FIGURE 4–55 The threshold voltage menu

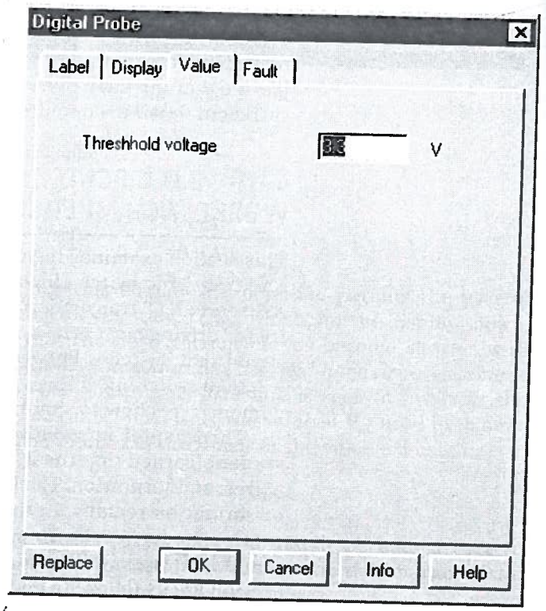
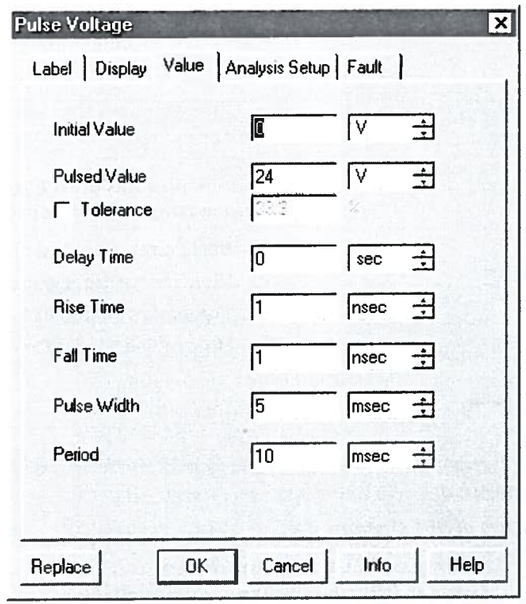


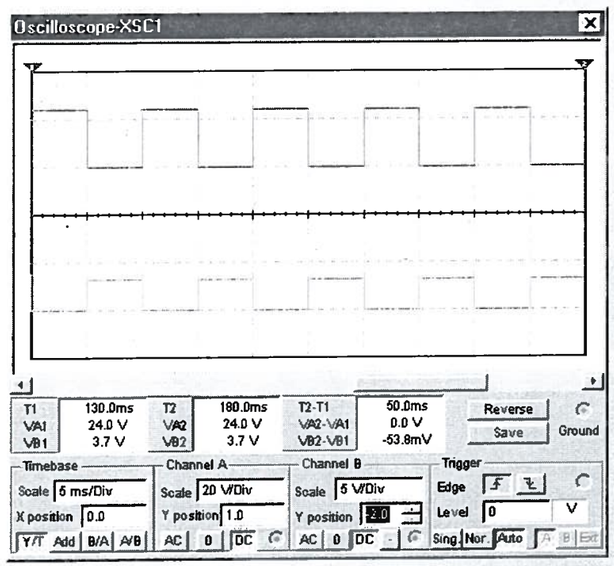
FIGURE 4–56 The menu for setting the pulse voltage values



The input pulse signal is set by double-clicking on the input pulse source. Next, click on value and set the initial and pulsed values. In this example, the initial value is 0 V and the pulsed value is 24 V. EWB also provides settings for the rise and fall time, pulse width, and period.

An oscilloscope (XSC1) is attached to the output to show that the signal is indeed switching. An example oscilloscope trace is provided in Figure 4–57.

FIGURE 4–57 The oscilloscope trace for the input signal and the output of the switching circuit



Is this the expected result? The input voltage is switching between 0 and +24 V. The output is switching between 0 and 3.3 V. It appears that the design objective has been met.

SUMMARY

This chapter has presented the basics of the BJT transistor. Students should have mastered those concepts and skills:

- Basic circuit analysis techniques.
- Identifying the transistor mode of operation.
- The basics of transistor curves.
- How to use the BJT switch in a circuit.

EXERCISES

SECTION 4–2

Theory of BJT Operation

4–1. In a certain transistor, the emitter current is 1.01 times as large as the collector current. If the emitter current is 12.12 mA, find the base current.

4–2. A (conventional) current of 26 μA flows out of the base of a certain transistor. The emitter current is 0.94 mA. What is the collector current and what kind of transistor is it (*npn* or *pnp*)? Draw a transistor symbol and label all current flows, showing directions and magnitudes.

4–3. In a certain transistor, 99.5% of the carriers injected into the base cross the collector–base junction. If the leakage current is 5.0 μA and the collector current is 22 mA, find

(a) the exact α,

(b) the emitter current, and

(c) the approximate α when I_{CBO} is neglected.

4–4. A germanium transistor has a surface leakage current of 1.4 μA and a reverse current due to thermally generated minority carriers of 1.2 nA at 10°C. If α = 0.992 and I_E = 0.8 mA, find I_C at 10°C and at 90°C. (Assume that surface leakage is independent of temperature.)

4–5. Using equation 4–2 and neglecting I_{CBO}, derive the following approximation: $I_B \approx (1 - \alpha)I_E$.

SECTION 4–3

Common-Base Characteristics

4–6. A certain transistor has the CB input characteristics shown in Figure 4–11. It is desired to hold I_E constant at 9.0 mA while V_{CB} is changed from 0 V to 25 V. What change in V_{BE} must accompany the change in V_{CB}?

4–7. A transistor has the CB input characteristics shown in Figure 4–11. If α = 0.95, find I_C when V_{BE} = 0.72 V and V_{CB} = 10 V.

SECTION 4–4

Common-Emitter Characteristics

4–8. A transistor has an α of 0.98 and a collector-to-base leakage current of 0.02 μA.

(a) Find its collector-to-emitter leakage current.

(b) Find the β of the transistor.

(c) Find I_C when I_B = 0.04 mA.

(d) Find the approximate I_C, neglecting leakage current.

4–9. A transistor has I_{CBO} = 0.1 μA and I_{CEO} = 16 μA. Find its α.

4–10. Derive the relation α = β/(β + 1). (*Hint:* Solve equation 4–8 for α.)

4–11. Under what condition is the approximation $I_{CEO} \approx \beta I_{CBO}$ valid?

4–12. A transistor has the CE output characteristics shown in Figure 4–20.

(a) Find the emitter current at V_{CE} = 5 V and I_B = 50 μA.

(b) Find the α at that point (neglecting leakage current).

4–13. An *npn* transistor has the CE input characteristics shown in Figure 4–19 and the CE output characteristics shown in Figure 4–20.

(a) Find I_B when V_{BE} = 0.7 V and V_{CE} = 20 V.

(b) Find the β of the transistor at V_{CE} = 6.0 V and I_B + 20μA (neglecting leakage current).

4–14. Using graphical methods, determine the approximate value of the Early voltage for the transistor whose CE output characteristics are shown in Figure 4–58.

4–15. In a certain experiment, the collector current of a transistor was measured at different values of collector-emitter voltage, while the base current was held constant. The results of the experiment are summarized in the following table:

I_B = 100 μA	
V_{CE}	I_C
5 V	15 mA
10 V	16 mA
15 V	17 mA
20 V	18 mA
I_B = 200 μA	
V_{CE}	I_C
5 V	30 mA
10 V	32 mA
15 V	34 mA
20 V	36 mA
I_B = 300 μA	
V_{CE}	I_C
5 V	45 mA
10 V	48 mA
15 V	51 mA
20 V	54 mA

Plot the experimental data and graphically determine approximate values for the following:

(a) β at V_{CE} = 8 V and I_B = 100 μA,

(b) β at V_{CE} = 14 V and I_B = 250 μA, and

(c) the Early voltage.

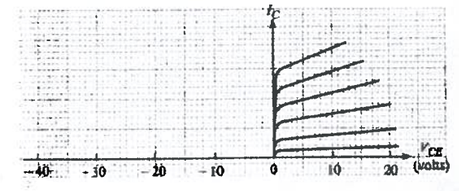


FIGURE 4–58 (Exercise 4–14)

SECTION 4–5

Common-Collector Characteristics

4–16. A certain transistor has the common-collector output characteristics shown in Figure 4–27. Neglecting leakage current, find approximate values for

(a) β at V_{CE} = 12.5 V and I_B = 20 μA,

(b) I_E at V_{CE} = 12.5 V and I_B = 45 μA, and

(c) α at V_{CE} = 2.5 V and I_B = 70 μA.

4–17. Prove that equation 4–16 is equivalent to $I_E = I_B/(1 - \alpha)$.

SECTION 4–6

Bias Circuits

4–18. Determine the equation for the load line of the circuit shown in Figure 4–59. Sketch the line and label the values of its intercepts.

4–19. In the circuit of Figure 4–59 find

(a) I_C when V_{CB} = 10 V, and

(b) V_{CB} when I_C = 1 mA.

4–20. In the circuit shown in Figure 4–60, find

(a) I_C when V_{BC} = 20 V, and

(b) V_{BC} when I_C = 4.2 mA.

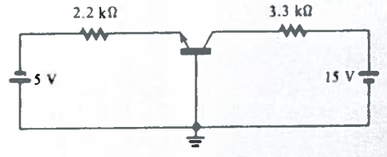


FIGURE 4–59 (Exercise 4–18)

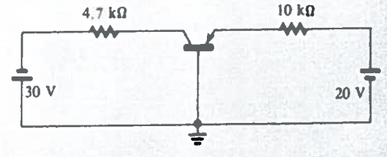


FIGURE 4–60 (Exercise 4–20)

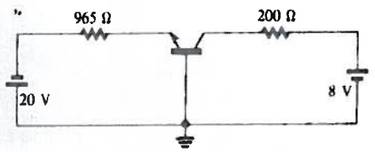


FIGURE 4–61 (Exercise 4–21)

4–21. The silicon transistor shown in Figure 4–61 has the CB output characteristics shown in Figure 4–62

(a) Draw the load line on the characteristics and graphically determine V_{CB} and I_C at the bias point.

(b) Determine the bias point without using the characteristic curves.

4–22. The transistor shown in Figure 4–63 is germanium.

(a) If $R_C = 1\ \text{k}\Omega$, what value of R_E will cause V_{BC} to equal 0 V?

(b) If $R_E = 1.5\ \text{k}\Omega$, what value of R_C will cause V_{BC} to equal 0 V?

4–23. In the circuit shown in Figure 4–64, find

(a) V_{CE} when $I_C = 1.5$ mA,

(b) I_C when $V_{CE} = 12$ V, and

(c) V_{CE} when $I_C = 0$.

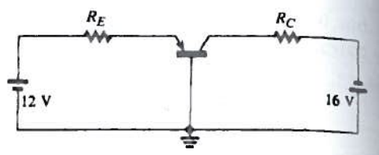


FIGURE 4–63 (Exercise 4–22)

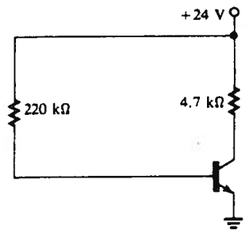


FIGURE 4–64 (Exercise 4–23)

4–24. In the circuit shown in Figure 4–65, find

(a) V_{EC} when $I_C = 12$ mA,

(b) I_C when $V_{EC} = 2.5$ V, and

(c) V_{EC} when $I_C = 0$.

4–25. The silicon transistor shown in Figure 4–66 has the CE output characteristics shown in Figure 4–67. Assume that $\beta = 105$.

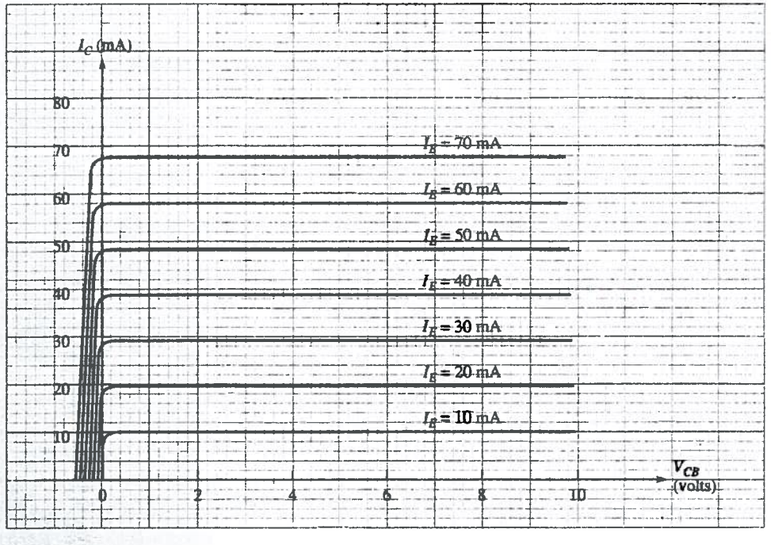


FIGURE 4–62 (Exercise 4–21)

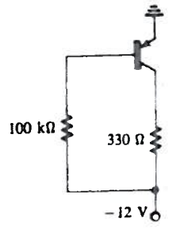


FIGURE 4–65 (Exercise 4–24)

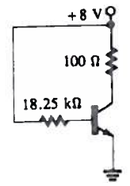


FIGURE 4–66 (Exercise 4–25)

(a) Draw the load line on the characteristics and graphically determine V_{CE} and I_C at the bias point.

(b) What is the approximate value of I_{CEO} for this transistor?

(c) Calculate V_{CE} and I_C at the bias point without using the characteristic curves.

4–26. Assuming that $\beta = 150$, find the bias point of the germanium transistor shown in Figure 4–68.

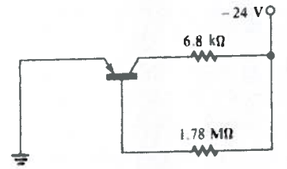


FIGURE 4–68 (Exercise 4–26)

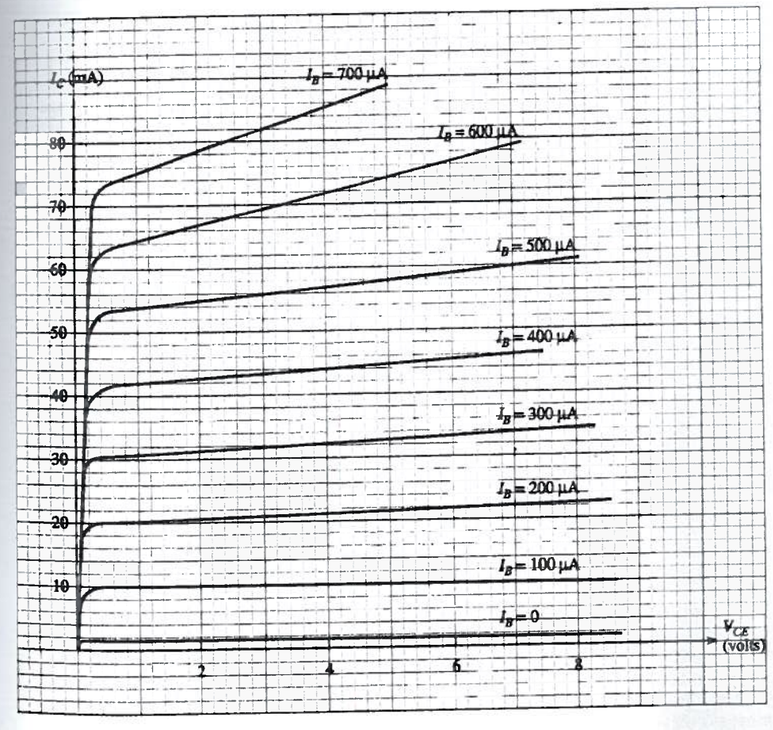


FIGURE 4–67 (Exercise 4–25)

4–27. What value of R_B in the circuit shown in Figure 4–69 will just cause the silicon transistor to be saturated, assuming that $\beta = 100$ and $V_{CE(sat)} = 0.3\,V$?

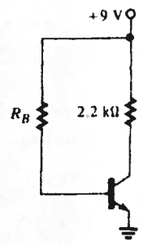


FIGURE 4–69 (Exercise 4–27)

4–28. Calculate the bias point of the silicon transistor shown in Figure 4–70. Assume that $\beta = 80$.

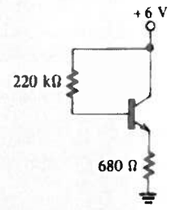


FIGURE 4–70 (Exercise 4–28)

4–29. Calculate the bias point of the silicon transistor shown in Figure 4–71. Assume that $\beta = 100$.

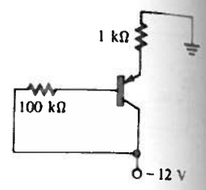


FIGURE 4–71 (Exercise 4–29)

4–30. Determine the bias configuration (CB, CE, or CC) of the transistor in each part of Figure 4–72.

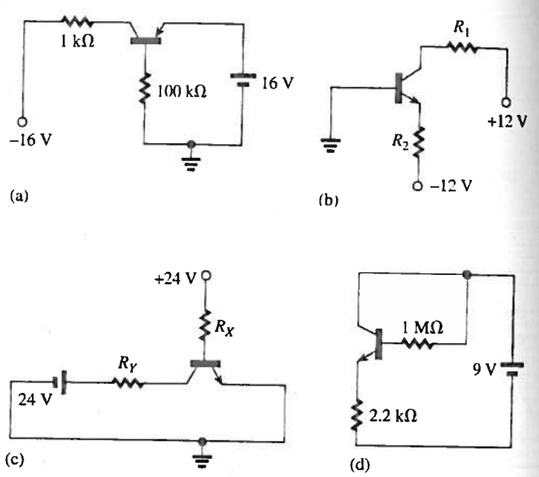


FIGURE 4–72 (Exercise 4–30)

DESIGN EXERCISES

4–31. (a) Design a bias circuit for an *npn* silicon transistor in a common-base configuration. The bias point should be $I_E = 2$ mA and $V_{CB} = 9$ V. Supply voltages are +20 V and −10 V. Use standard-valued resistors with 5% tolerance and draw a schematic diagram of your design.

(b) Calculate the range of possible values that the bias point could have, taking the resistor tolerances into consideration.

4–32. (a) Design a bias circuit for a *pnp* silicon transistor in a common-emitter configuration. The nominal β of the transistor is 80 and the supply voltage is −24 V. The bias point is to be $I_C = 5$ mA, and $V_{CE} = -10$ V. Use standard-valued resistors with 10% tolerance and draw a schematic diagram of your design.

(b) Calculate the actual bias point assuming the 10% resistors have their nominal values.

(c) Calculate the range of possible values that the bias point could have if the value of β changed over the range from 50 to 100. Assume the resistors have their nominal values.

4–33. (a) Design a bias circuit for an *npn* silicon transistor in a common-collector configuration. The nominal β for the transistor is 100, and the supply voltage is 30 V. The bias point is to be $I_C = 10$ mA, and $V_{CE} = 12$ V. Use standard-valued resistors having 5% tolerance and draw a schematic diagram of your design.

(b) Calculate the *minimum* value that V_{CE} could have if *both* the resistor tolerances and a variation in β from 60 to 120 are taken into account. *Hint*: Use equations 4–28 to derive the expression

$$V_{CE} = V_{CC} - \frac{(V_{CC} - V_{BE})}{\frac{R_B}{(\beta + 1)R_E} + 1}$$

4–34. (a) Design a bias circuit for an *npn* silicon transistor having a nominal β of 100, to be used in a common-emitter configuration. The bias point is to be $I_C = 1$ mA, and $V_{CE} = 5$ V. The supply voltage is 15 V. Use standard-valued 5% resistors and draw a schematic diagram of your design.

(b) Calculate the possible range of values of the bias point taking into consideration *both* the resistor tolerances and a possible variation in β from 30 to 150. Interpret and comment on your results.

SECTION 4–8

The BJT Inverter (Transistor Switch)

4–35. The input to the circuit shown in Figure 4–73 alternates between 0 V and 10 V. If the silicon transistor has a β of 120, verify that the circuit operates as an inverter.

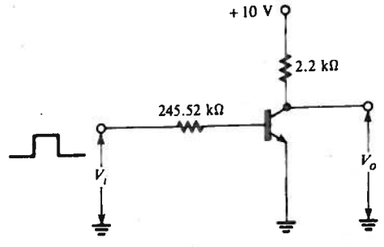


FIGURE 4–73 (Exercise 4–35)

4–36. What would be the output voltages from the inverter in Figure 4–73 if

(a) the input voltage levels were changed to −5 V and +10 V?

(b) the input voltage levels were changed to 0 V and +15 V?

(c) the β of the transistor were changed to 150?

4–37. A transistor inverter is to be designed using a silicon transistor whose β may vary from 60 to 120. If the series base resistance is to be 100 kΩ, what should be the value of R_C? Assume that $V_{CC} = V_{IH} = 4.5$ V.

4–38. What is the minimum value of β for which the silicon transistor in Figure 4–74 will operate satisfactorily as an inverter?

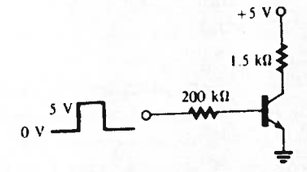


FIGURE 4–74 (Exercise 4–38)

SECTION 4–9

Transistor Types, Ratings, and Specifications

Note: In Exercises 4–39 through 4–40, refer to the manufacturer's specification sheets given in Section 4–9.

4–39. The input to the 2N2222,A, transistor in Figure 4–75 is a square wave that alternates between ±V volts. Assuming that no base current flows when the input is at −V volts (so there is no drop across R_B), what is the maximum safe value for V? Assume that a safe value for V is one that does not exceed 80% of the manufacturer's rated maximum.

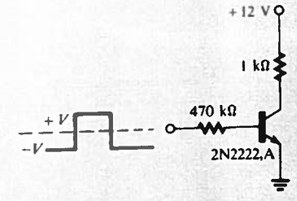


FIGURE 4–75 (Exercise 4–39)